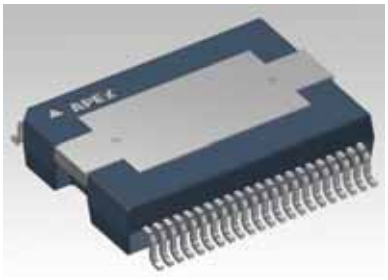
SA53

Switching Amplifier

RoHS COMPLIANT

FEATURES



- Low Cost Intelligent Switching Amplifier
- Directly Connects to Most Embedded Microcontrollers and Digital Signal Controllers
- Integrated Gate Driver Logic with Dead-time Generation and Shoot-through Prevention
- Wide Power Supply Range (8.5 V To 60 V)
- Over 10A Peak Output Current per Phase
- Independent Current Sensing for each Output
- User Programmable Cycle-by-Cycle Current Limit Protection
- Over-Current and Over-Temperature Warning Signals

APPLICATIONS

- Bidirectional DC Brush Motors
- 2 Unidirectional DC Brush Motors
- 2 Independent Solenoid Actuators
- Stepper Motors

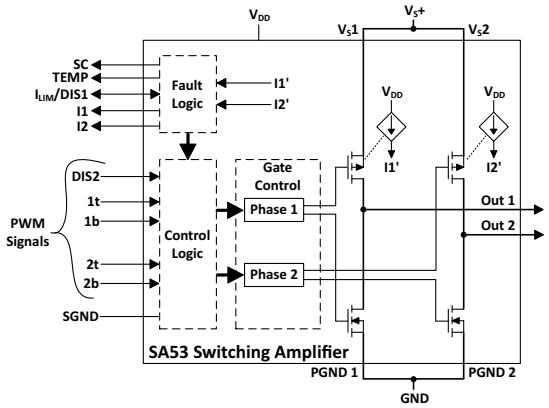
DESCRIPTION

The SA53 is a fully integrated switching amplifier designed primarily to drive DC brush motors. Two independent half bridges provide over 10 amperes peak output current under microcontroller or DSC control. Thermal and short circuit monitoring is provided, which generates fault signals for the microcontroller to take appropriate action.

Additionally, cycle-by-cycle current limit offers user programmable hardware protection independent of the microcontroller. Output current is measured using an innovative low loss technique. The SA53 is built using a multi-technology process allowing CMOS logic control and complementary DMOS output power devices on the same IC. Use of P-channel high side FETs enables 60V operation without bootstrap or charge pump circuitry.

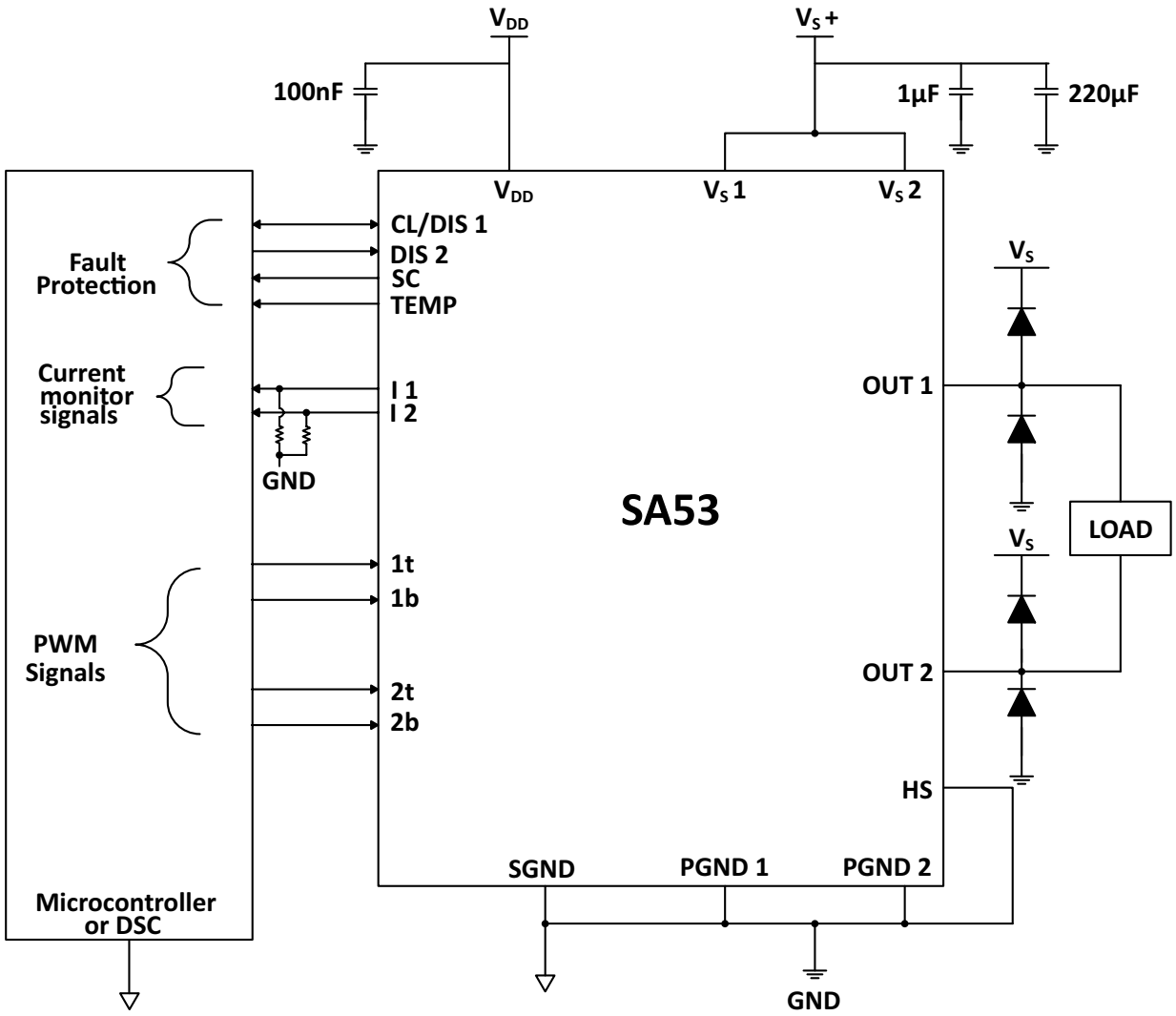
The HSOP surface mount package balances excellent thermal performance with the advantages of a low profile surface mount package.

Figure 1: Block Diagram



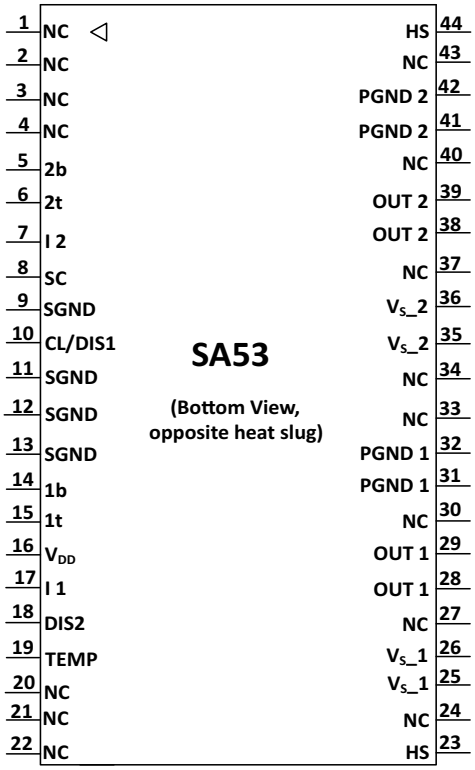
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Case tied to Pins 23 and 44. Allow no current in case. Bypassing of supplies is required.

Pin Number	Name	Description
5	2b	Logic high commands phase 2 lower (bottom) FET to turn on.
6	2t	Logic high commands phase 2 upper (top) FET to turn on.
7	I 2	Phase 2 current sense output. Outputs a current proportional to I_D of the upper (top) FET of channel 2. Connect to a sense resistor to SGND to monitor current.
8	SC	Short circuit output. When a short circuit condition is experienced on either channel, this pin will go high for 200ns. This does not disable the outputs.
9, 11, 12, 13	SGND	Signal ground. Reference all logic circuitry to these pins. Connect to PGND 1 and PGND 2 as close to the amplifier as possible.
10	CL/DIS1	Logic high places both outputs in a high impedance state. Pulling to logic low disables cycle-by-cycle current limit. If unconnected, cycle-by-cycle current limit will be allowed to operate.
14	1b	Logic high commands phase 1 lower (bottom) FET to turn on.
15	1t	Logic high commands phase 1 upper (top) FET to turn on.
16	Vdd	Voltage supply for logic circuit. Connect 5 V supply. The ground terminal of the supply must be connected to SGND.

Pin Number	Name	Description
17	I 1	Phase 1 current sense output. Outputs a current proportional to I_D of the upper (top) FET of channel 1. Connect to a sense resistor to SGND to monitor current.
18	DIS2	Logic high places both outputs in a high impedance state. This pin may be left unconnected.
19	TEMP	This pin will go logic high when the die temperature reaches 135°C. This does not disable the outputs.
23, 44	HS	These pins are internally connected to the heat slug. Connect to PGND. Neither the heatslug nor these pins should carry current.
25, 26	Vs 1	Voltage supply for channel 1.
28, 29	OUT 1	The output connection for channel 1.
31, 32	PGND 1	Power ground. These pins are directly connected to the bottom FET of channel 1. Connect to SGND and PGND 2 as close to the amplifier as possible.
35, 36	Vs 2	Voltage supply for channel 2.
38, 39	OUT 2	The output connection for channel 2.
41, 42	PGND 2	Power ground. These pins are directly connected to the bottom FET of channel 2. Connect to SGND and PGND 1 as close to the amplifier as possible.
All Others	NC	No connection.

PIN DESCRIPTIONS

V_S: Supply voltage for the output transistors. These pins require decoupling (1µF capacitor with good high frequency characteristics is recommended) to the PGND pins. The decoupling capacitor should be located as close to the V_S and PGND pins as possible. Additional capacitance will be required at the V_S pins to handle load current peaks and potential motor regeneration. Refer to the applications section of this datasheet for additional discussion regarding bypass capacitor selection. Note that V_S pins 25-26 carry only the phase 1 supply current. Pins 35-36 carry supply current for phase 2. Phase 1 may be operated at a different supply voltage from phase 2. Both V_S voltages are monitored for undervoltage conditions.

OUT 1, OUT 2: These pins are the power output connections to the load. NOTE: When driving an inductive load, it is recommended that two Schottky diodes with good switching characteristics (fast t_{RR} specs) be connected to each pin so that they are in parallel with the parasitic back-body diodes of the output FETs.

PGND: Power Ground. This is the ground return connection for the output FETs. Return current from the load flows through these pins. PGND is internally connected to SGND through a resistance of a few ohms. See section 2.1 of this datasheet for more details.

SC: Short Circuit output. If a condition is detected on any output which is not in accordance with the input commands, this indicates a short circuit condition and the SC pin goes high. The SC signal is blanked for approximately 200ns during switching transitions but in high current applications, short glitches may appear on the SC pin. A high state on the SC output will not automatically disable the device. The SC pin includes an internal 12 kΩ series resistor.

1b, 2b: These Schmitt triggered logic level inputs are responsible for turning the associated bottom, or lower N-channel output FETs on and off. Logic high turns the bottom N-channel FET on, and a logic low turns the low side N-channel FET off. If 1b or 2b is high at the same time that a corresponding 1t or 2t input is high, protection circuitry will turn off both FETs in order to prevent shoot-through on that output phase. Protection circuitry also includes a dead-time generator, which inserts dead time in the outputs in the case of simultaneous switching of the top and bottom input signals.

1t, 2t: These Schmitt triggered logic level inputs are responsible for turning the associated top side, or upper

P-channel FET outputs on and off. Logic high turns the top P-channel FET on, and a logic low turns the top P-channel FET off.

I1, I2: Current sense pins. The SA53 supplies a positive current to these pins which is proportional to the cur rent flowing through the top side P-channel FET for that phase. Commutating currents flowing through the backbody diode of the P-channel FET or through external Schottky diodes are not registered on the current sense pins. Nor do currents flowing through the low side N-channel FET, in either direction, register at the current sense pins. A resistor connected from a current sense pin to SGND creates a voltage signal representation of the phase current that can be monitored with ADC inputs of a processor or external circuitry.

The current sense pins are also internally compared with the current limit threshold voltage reference, Vth. If the voltage on any current sense pin exceeds Vth, the cycle by cycle current limit circuit engages. Details of this functionality are described in the applications section of this datasheet.

CL/DIS1: This pin is directly connected to the disable circuitry of the SA53. Pulling this pin to logic high places OUT 1 and OUT 2 in a high impedance state. This pin is also connected internally to the output of the current limit latch through a 12 kΩ resistor and can be monitored to observe the function of the cycle-by-cycle current limit feature. Pulling this pin to a logic low effectively disables the cycle-by-cycle current limit feature.

SGND: This is the ground return connection for the V_{DD} logic power supply pin. All internal analog and logic circuitry is referenced to this pin. PGND is internally connected to GND through a resistance of a few ohms. However, it is highly recommended to connect the GND pin to the PGND pins externally as close to the device as possible. Failure do to this may result in oscillations on the output pins during rising or falling edges.

V_{DD}: This is the connection for the 5V power supply, and provides power for the logic and analog circuitry in the SA53. This pin requires decoupling (at least 0.1µF capacitor with good high frequency characteristics is recommended) to the SGND pin.

DIS2: The DIS2 pin is a Schmitt triggered logic level input that places OUT 1 and OUT 2 in a high impedance state when pulled high. DIS2 has an internal 12 kΩ pull-down resistor and may therefore be left unconnected.

TEMP: This logic level output goes high when the die temperature of the SA53 reaches approximately 135°C. This pin WILL NOT automatically disable the device. The TEMP pin includes a 12 kΩ series resistor.

HS: These pins are internally connected to the thermal slug on the reverse of the package. They should be connected to GND. Neither the heat slug nor these pins should be used to carry high current.

NC: These “no-connect” pins should be left unconnected.

SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_S		60	V
Supply Voltage	V_{DD}		5.5	V
Logic Input Voltage		(-0.5)	(V_{DD}+0.5)	V
Output Current, peak, 10ms [1]	I_O		10	A
Power Dissipation, avg. 25°C [1]	P_D		100	W
Temperature, pin solder, 10s max.			260	°C
Temperature, junction [1]	T_J		150	°C
Temperature Range, storage		-65	+125	°C
Operating Temperature Range, case	T_C	-25	+85	°C

1. Long term operation at elevated temperature will result in reduced product life. De-rate internal power dissipation to achieve high MTBF.

LOGIC

Parameter	Test Conditions	Min	Typ	Max	Units
Input Low				1	V
Input High		1.8			V
Output Low				0.3	V
Output High		3.7			V
Output Current (SC, Temp, CL/ DIS1)			50		mA

POWER SUPPLY

Parameter	Test Conditions	Min	Typ	Max	Units
V_S		UVLO	50	60	V
V_S Undervoltage Lockout, (UVLO)			8.3		V
V_{DD}		4.5		5.5	V
Supply Current, V_S	20 kHz (One phase switching at 50% duty cycle), V_S=50V, V_{DD}=5V		25	30	mA
Supply Current, V_{DD}	20 kHz (One phase switching at 50% duty cycle), V_S=50V, V_{DD}=5.5V		5	6.5	mA

CURRENT LIMIT

Parameter	Test Conditions	Min	Typ	Max	Units
Current Limit Threshold (Vth)			3.75		V
Vth Hysteresis			100		mV

OUTPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Current, continuous	25°C Case Temperature	3			A
Rising Delay, TD (rise)	See Figure 20		270		ns
Falling Delay, TD (fall)	See Figure 20		270		ns
Disable Delay, TD (dis)	See Figure 20		200		ns
Enable Delay, TD (dis)	See Figure 20		200		ns
Rise Time, t (rise)	See Figure 21		50		ns
Fall Time, t (fall)	See Figure 21		50		ns
On Resistance Sourcing (P-Channel)	5A Load		400		mΩ
On Resistance Sinking (N-Channel)	5A Load		400		mΩ

THERMAL

Parameter	Test Conditions	Min	Typ	Max	Units
Thermal Warning			135		°C
Thermal Warning Hysteresis			40		°C
Resistance, junction to case	Full temp range		1.25	1.5	°C/W
Temperature Range, case	Meets Specs	-25		+85	°C

Note: Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

TYPICAL PERFORMANCE GRAPHS

Figure 4: V_S Supply Current

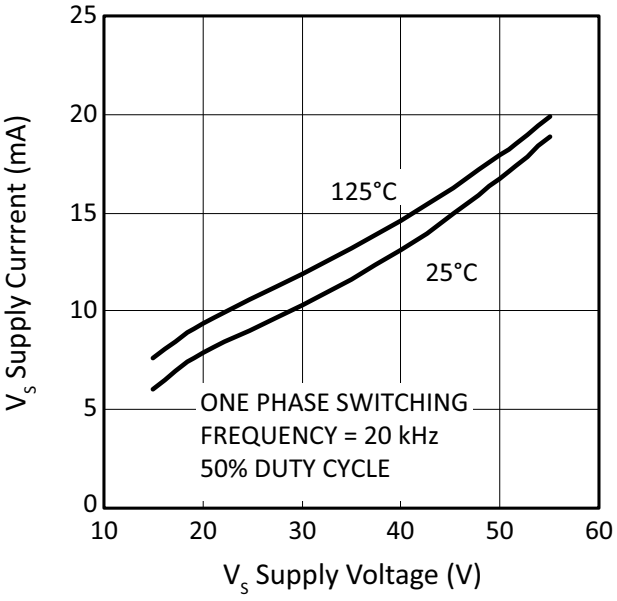


Figure 5: V_S Supply Current

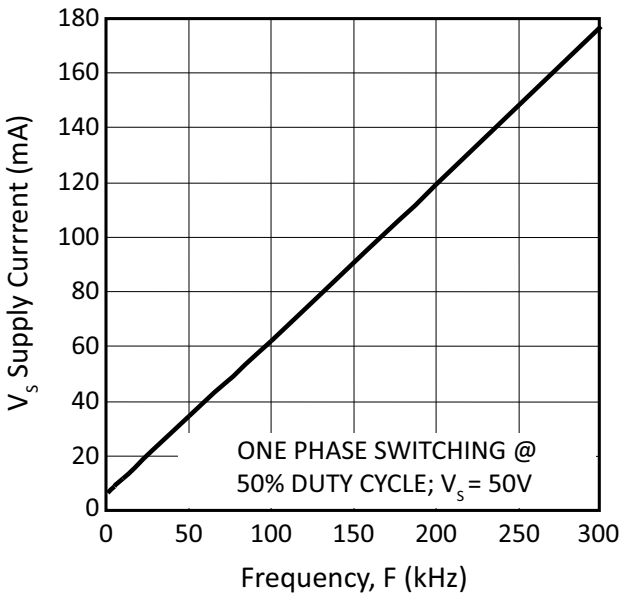


Figure 6: Current Sense

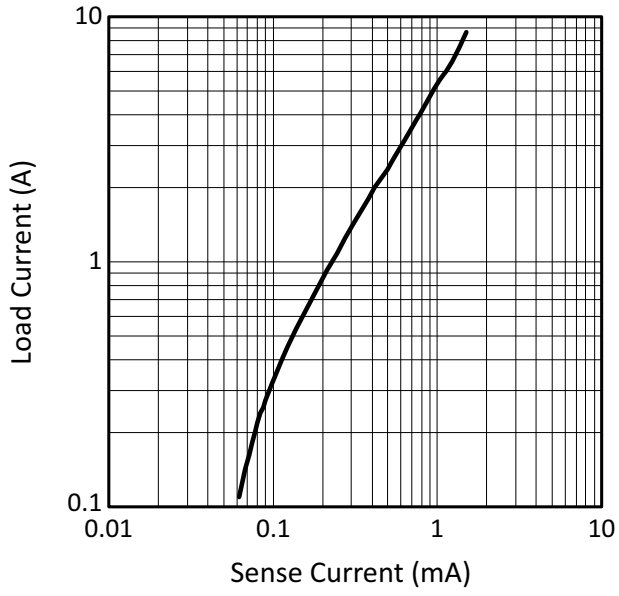


Figure 7: V_{DD} Supply Current

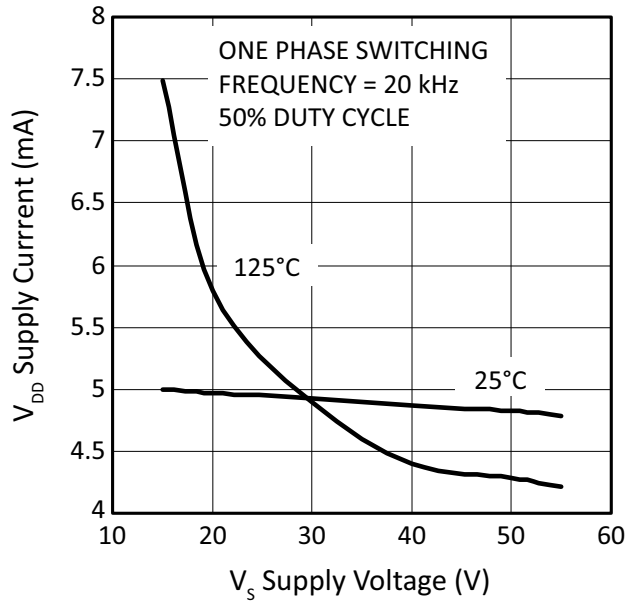


Figure 8: V_{DD} Supply Current

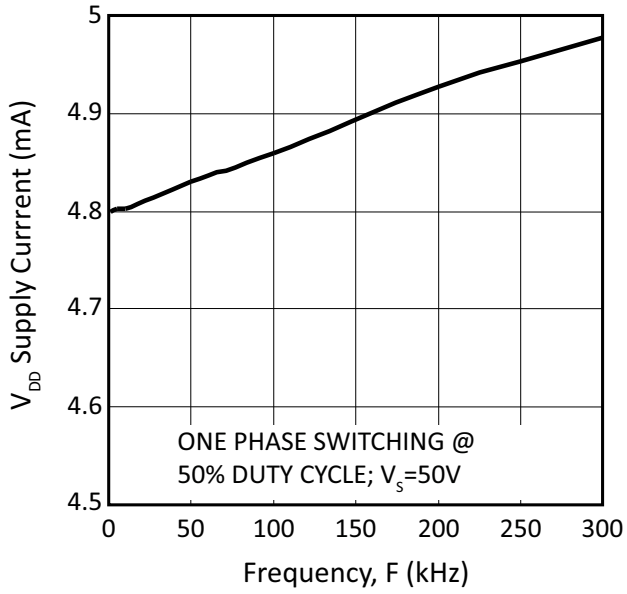


Figure 9: Power Derating

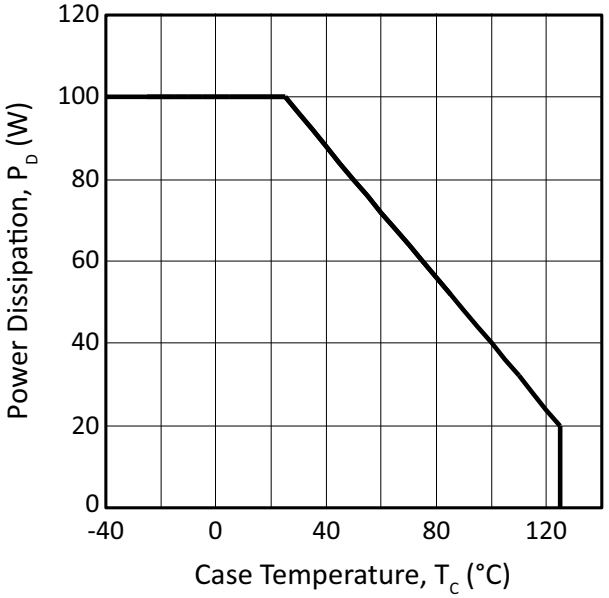


Figure 10: On Resistance - Bottom FET

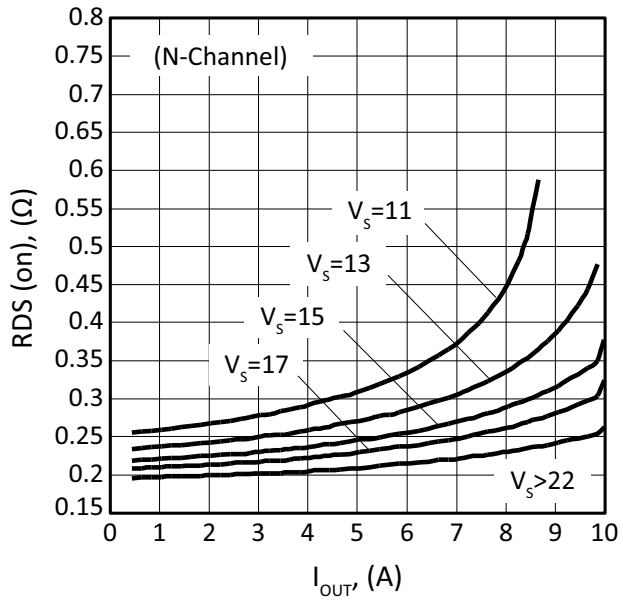


Figure 11: On Resistance - Top FET

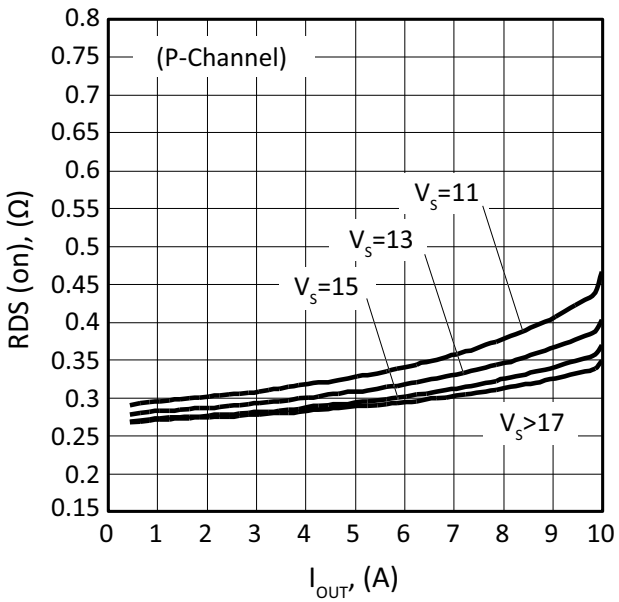


Figure 12: Diode Forward Voltage - Bottom FET

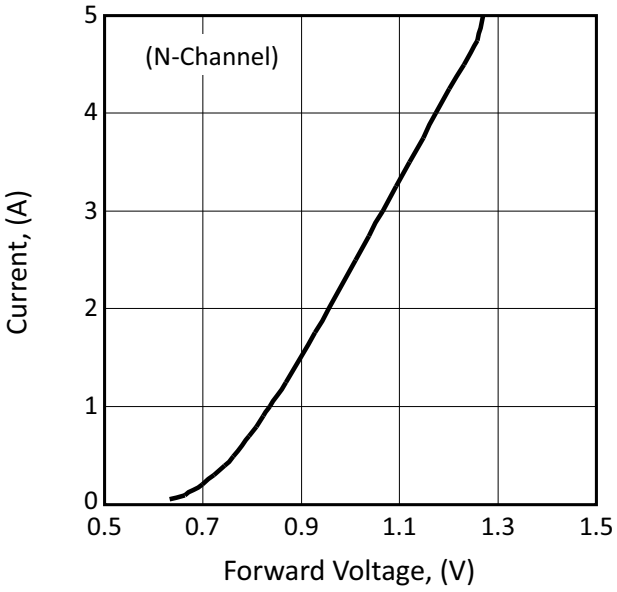
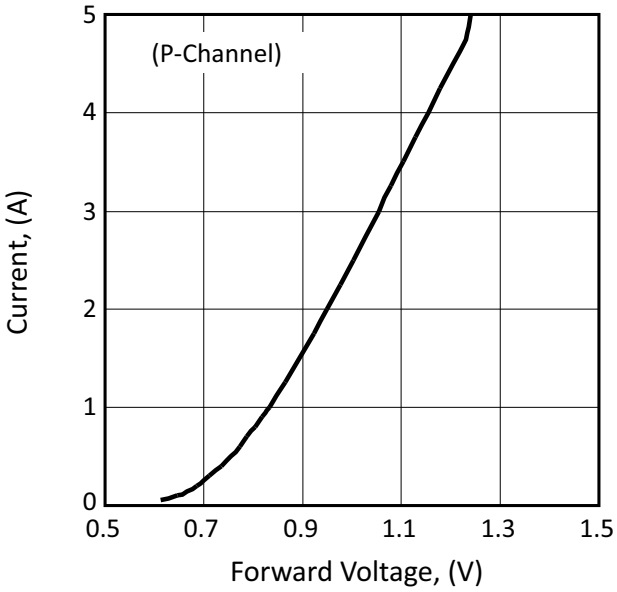


Figure 13: Diode Forward Voltage - Top FET



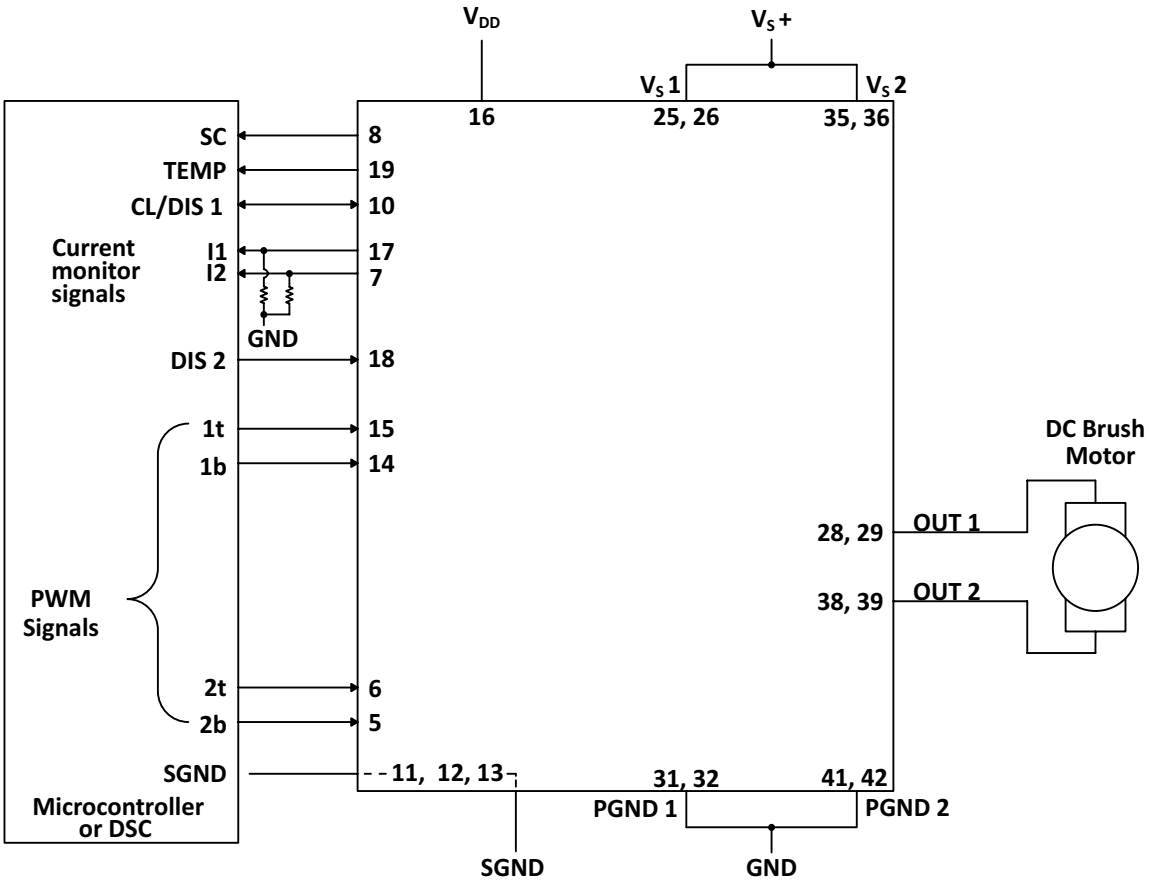
GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

SA53 OPERATION

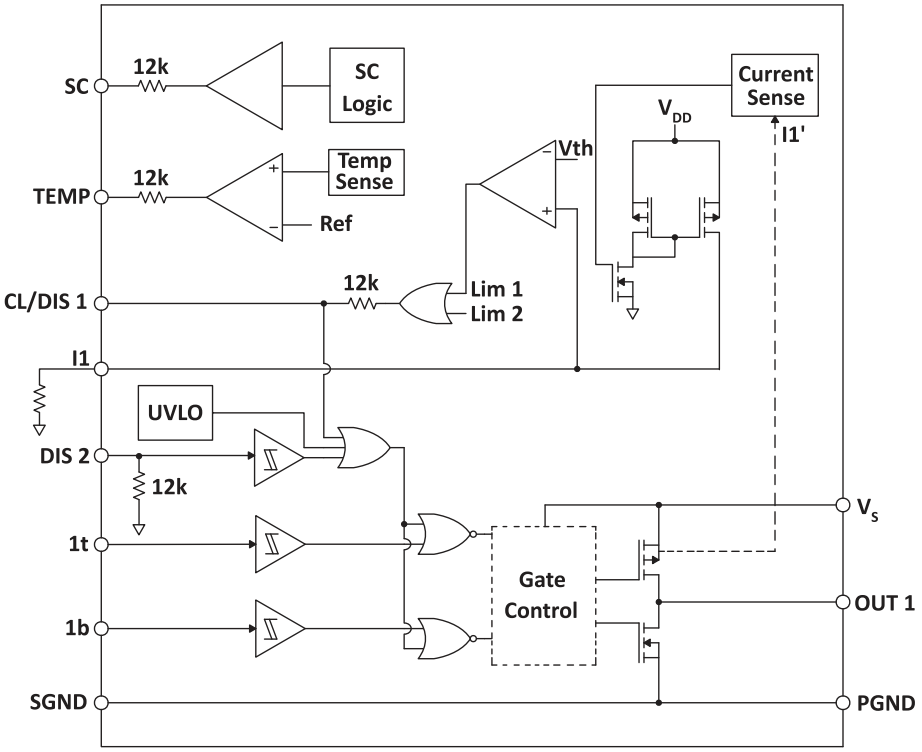
The SA53 is designed primarily to drive DC brush motors. However, it can be used for any application requiring two high current outputs. The signal set of the SA53 is designed specifically to interface with a DSP or microcontroller. A typical system block diagram is shown in the figure below. Over-temperature, Short-Circuit and Current Limit fault signals provide important feedback to the system controller which can safely disable the output drivers in the presence of a fault condition. High side current monitors for both phases provide performance information which can be used to regulate or limit torque.

Figure 14: System Diagram



The block diagram in Figure 15 illustrates the features of the input and output structures of the SA53. For simplicity, a single phase is shown.

Figure 15: Input And Output Structures For A Single Phase Layout Considerations



TRUTH TABLE

At, Bt, Ct	Ab, Bb, Cb	Ia, Ib, Ic	I_{LIM}/ DIS1	DIS2	Out A, Out B, Out C	Comments
0	0	X	X	X	High-Z	Top and Bottom output FETs for that phase are turned off.
0	1	$<V_{th}$	0	0	PGND	Bottom output FET for that phase is turned on.
1	0	$<V_{th}$	0	0	VS	Top output FET for that phase is turned on.
1	1	X	X	X	High-Z	Both output FETs for that phase are turned off.
X	X	$>V_{th}$	1	X	High-Z	Voltage on Ia, Ib, or Ic has exceeded Vth, which causes I_{LIM}/DIS1 to go high. This internally disables Top and Bottom output FETs for ALL phases.
X	X	X	X	1	High-Z	DIS2 pin pulled high, which disables all outputs.
X	X	X	Pulled High	X	High-Z	Pulling the I_{LIM}/DIS1 pin high externally acts as a second disable input, which disables ALL output FETs.
X	X	X	Pulled Low	0	Determined by PWM inputs	Pulling the I_{LIM}/DIS1 pin low externally disables the cycle-by-cycle current limit function. The state of the outputs is strictly a function of the PWM inputs.
X	X	X	X	X	High-Z	If V_S is below the UVLO threshold all output FETs will be disabled.

Output traces carry signals with very high dV/dt and dI/dt. Proper routing and adequate power supply bypassing ensures normal operation. Poor routing and bypassing can cause erratic and low efficiency operation as well as ringing at the outputs.

The V_S supply should be bypassed with a surface mount ceramic capacitor mounted as close as possible to the V_S pins. Total inductance of the routing from the capacitor to the V_S and GND pins must be kept to a minimum to prevent noise from contaminating the logic control signals. A low ESR capacitor of at least 25µF per ampere of output current should be placed near the SA53 as well. Capacitor types rated for switching applications are the only types that should be considered.

The bypassing requirements of the V_{DD} supply are less stringent, but still necessary. A 0.1µF to 0.47µF surface mount ceramic capacitor (X7R or NPO) connected directly to the V_{DD} pin is sufficient. SGND and PGND pins are connected internally. However, these pins must be connected externally in such a way that there is no motor current flowing in the logic and signal ground traces as parasitic resistances in the small signal routing can develop sufficient voltage drops to erroneously trigger input transitions. Alternatively, a ground plane may be separated into power and logic sections connected by a pair of back to back Schottky diodes. This isolates noise between signal and power ground traces and prevents high currents from passing between the plane sections.

Unused area on the top and bottom PCB planes should be filled with solid or hatched copper to minimize inductive coupling between signals. The copper fill may be left unconnected, although a ground plane is recommended.

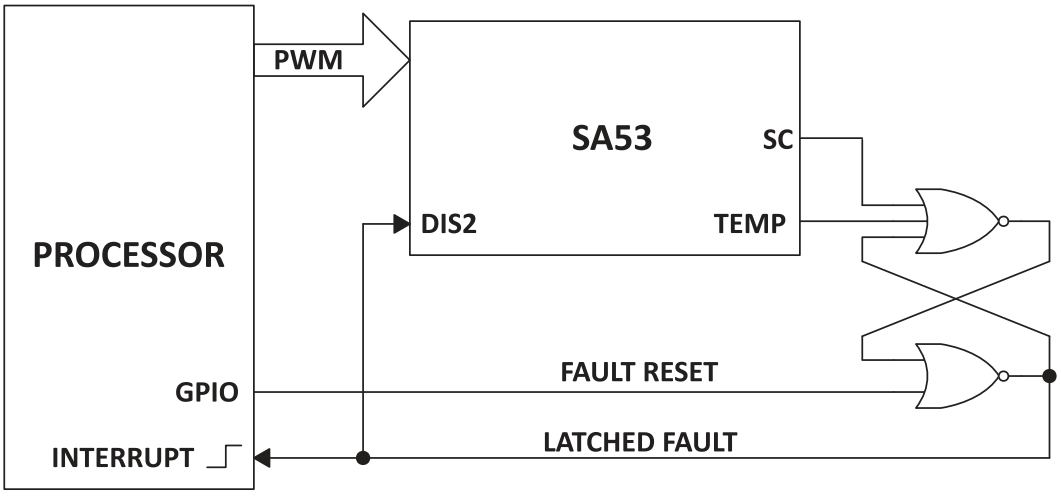
FAULT INDICATIONS

In the case of either an over-temperature or short circuit fault, the SA53 will take no action to disable the outputs. Instead, the SC and TEMP signals are provided to an external controller, where a determination can be made regarding the appropriate course of action. In most cases, the SC pin would be connected to a FAULT input on the processor, which would immediately disable its PWM outputs. The TEMP fault does not require such an immediate response, and would typically be connected to a GPIO, or Keyboard Interrupt pin of the processor. In this case, the processor would recognize the condition as an external interrupt, which could be processed in software via an Interrupt Service Routine. The processor could optionally bring all inputs low, or assert a high level to either of the disable inputs on the SA53.

Figure 16 shows an external SR flip-flop which provides a hard wired shutdown of all outputs in response to a fault indication. An SC or TEMP fault sets the latch, pulling the disable pin high. The processor clears the latched condition with a GPIO. This circuit can be used in safety critical applications to remove software from the fault-shutdown loop, or simply to reduce processor overhead.

In applications which may not have available GPIO, the TEMP pin may be externally connected to the adjacent DIS2 pin. If the device temperature reaches ~135°C all outputs will be disabled, de-energizing the motor. The SA53 will re-energize the motor when the device temperature falls below approximately 95°C. The TEMP pin hysteresis is wide to reduce the likelihood of thermal oscillations which can greatly reduce the life of the device.

Figure 16: External Fault Latch Circuit



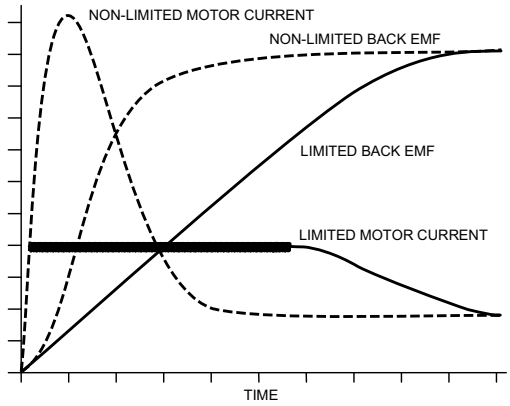
UNDER-VOLTAGE LOCKOUT

The undervoltage lockout condition results in the SA53 unilaterally disabling all output FETs until V_S is above the UVLO threshold indicated in the spec table. There is no external signal indicating that an undervoltage lockout condition is in progress. The SA53 has two V_S connections: one for phase 1 and another for phase 2. The supply voltages on these pins need not be the same, but the UVLO will engage if either is below the threshold. Hysteresis on the UVLO circuit prevents oscillations with typical power supply variations.

CURRENT SENSE

External power shunt resistors are not required with the SA53. Forward current in each top, P-channel output FET is measured and mirrored to the respective current sense output pin, Ia, Ib and Ic. By connecting a resistor between each current sense pin and a reference, such as ground, a voltage develops across the resistor that is proportional to the output current for that phase. An ADC can monitor the voltages on these resistors for protection or for closed loop torque control in some application configurations. The current sense pins source current from the V_{DD} supply. Headroom required for the current sense circuit is approximately 0.5V. The nominal scale factor for each proportional output current is shown in the typical performance plot on page 8 of this datasheet.

Figure 17: Start-Up Voltage and Current



CYCLE-BY-CYCLE CURRENT LIMIT

In applications where the current in the motor is not directly controlled, both the average current rating of the motor and the inrush current must be considered when selecting a proper amplifier. For example, a 1A continuous motor might require a drive amplifier that can deliver well over 10A peak in order to survive the inrush condition at startup.

Because the output current of each upper output FET is measured, the SA53 is able to provide a very robust current limit scheme. This enables the SA53 to safely and easily drive virtually any DC brush motor through a startup inrush condition. With limited current, the starting torque and acceleration are also limited. The plot in Figure 17 shows starting current and back EMF with and without current limit enabled.

If the voltage of any of the two current sense pins exceeds the current limit threshold voltage (Vth), all outputs are disabled. After all current sense pins fall below the Vth threshold voltage AND the offending phase's top side input goes low, the output stage will return to an active state on the rising edge of ANY top side input command signal (1t or 2t). With most commutation schemes, the current limit will reset each pwm cycle. This scheme regulates the peak current in each phase during each pwm cycle as illustrated in the timing diagram below. The ratio of average to peak current depends on the inductance of the motor winding, the back EMF developed in the motor, and the width of the pulse.

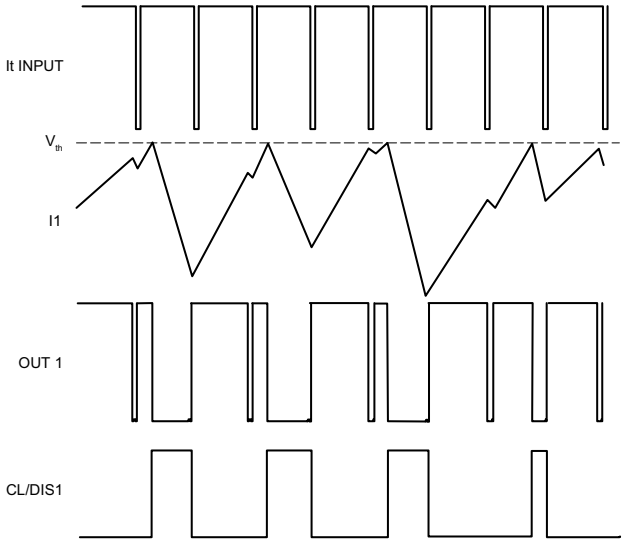
Figure 18 illustrates the current limit trigger and reset sequence. Current limit engages and CL/DIS1 goes high when any current sense pin exceeds Vth. Notice that the moment at which the current sense signal exceeds the Vth threshold is asynchronous with respect to the input PWM signal. The difference between the PWM period and the motor winding L/R time constant will often result in an audible beat frequency sometimes called a sub-cycle oscillation.

This oscillation can be seen on the CL/DIS1 pin waveform in Figure 18. Input signals commanding 0% or 100% duty cycle may be incompatible with the current limit feature due to the absence of rising edges of 1t and 2t except when commutating phases. At high RPM, this may result in poor performance. At low RPM, the motor may stall if the current limit trips and the motor current reaches zero without a commutation edge which will typically reset the current limit latch.

The current limit feature may be disabled by tying the CL/Dis1 pin to GND. The current sense pins will continue to provide top FET output current information.

Typically, the current sense pins source current into grounded resistors which provide voltages to the current limit comparators. If instead the current limit resistors are connected to a voltage output DAC, the current limit can be controlled dynamically from the system controller. This technique essentially reduces the current limit threshold voltage to (Vth-VDAC). During expected conditions of high torque demand, such as start-up or reversal, the DAC can adjust the current limit dynamically to allow periods of high current. In normal operation when low current is expected, the DAC output voltage can increase, reducing the current limit setting to provide more conservative fault protection.

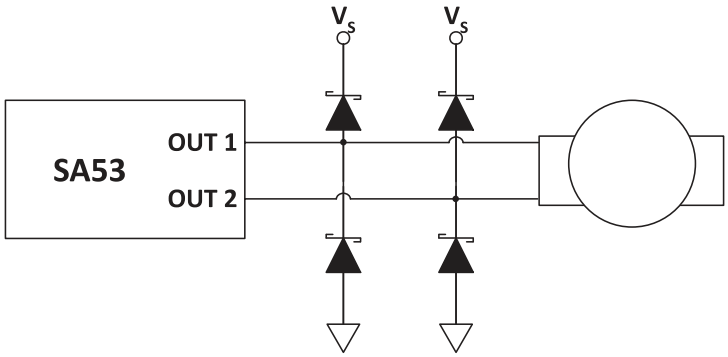
Figure 18: Current Limit Waveforms



EXTERNAL FLYBACK DIODES

External fly-back diodes will offer superior reverse recovery characteristics and lower forward voltage drop than the internal back-body diodes. In high current applications, external flyback diodes can reduce power dissipation and heating during commutation of the motor current. Reverse recovery time and capacitance are the most important parameters to consider when selecting these diodes. Ultra-fast rectifiers offer better reverse recovery time and Schottky diodes typically have low capacitance. Individual application requirements will be the guide when determining the need for these diodes and for selecting the component which is most suitable.

Figure 19: Schottky Diodes



POWER DISSIPATION

The thermally enhanced package of the SA53 allows several options for managing the power dissipated in the three output stages. Power dissipation in traditional PWM applications is a combination of output power dissipation and switching losses. Output power dissipation depends on the quadrant of operation and whether external flyback diodes are used to carry the reverse or commutating currents. Switching losses are dependent on the frequency of the PWM cycle as described in the typical performance graphs.

Figure 20: Timing Diagrams

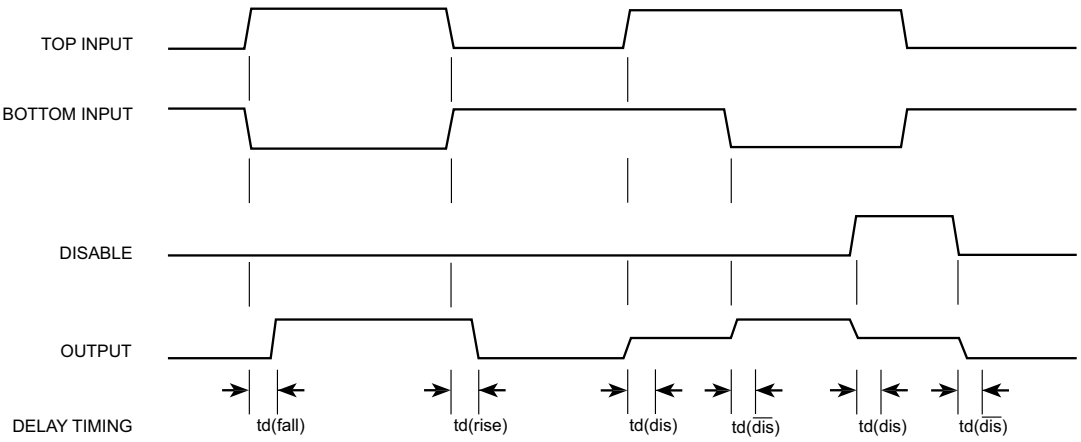
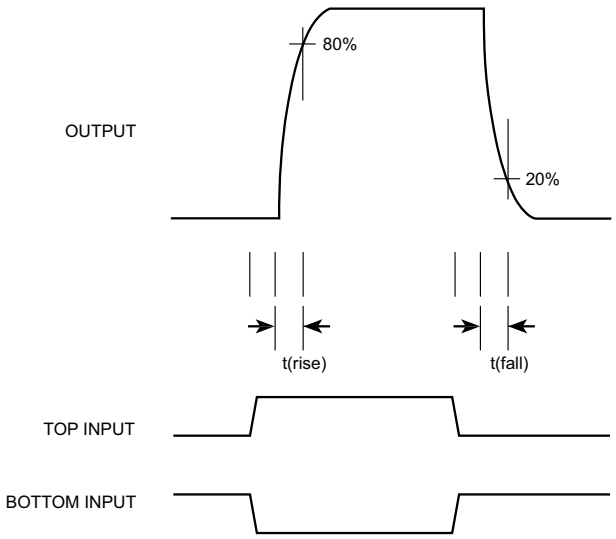


Figure 21: Output Response



PACKAGE OPTIONS

Part Number	Apex Package Style	Description
SA53	HU	44-pin HSOP Slug Up

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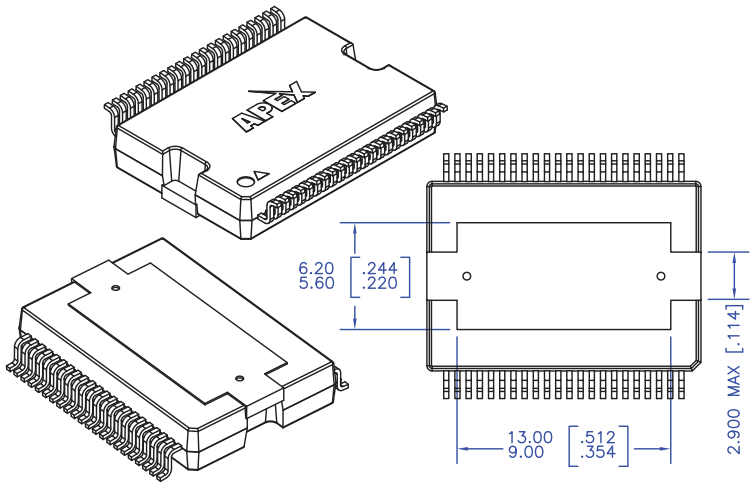
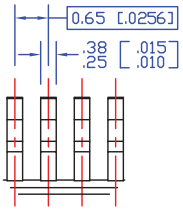
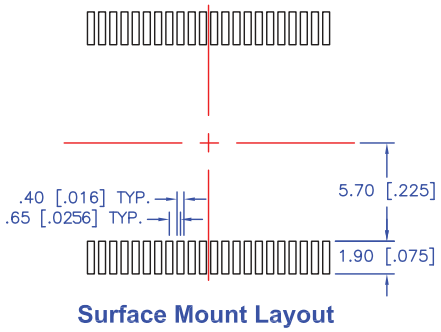
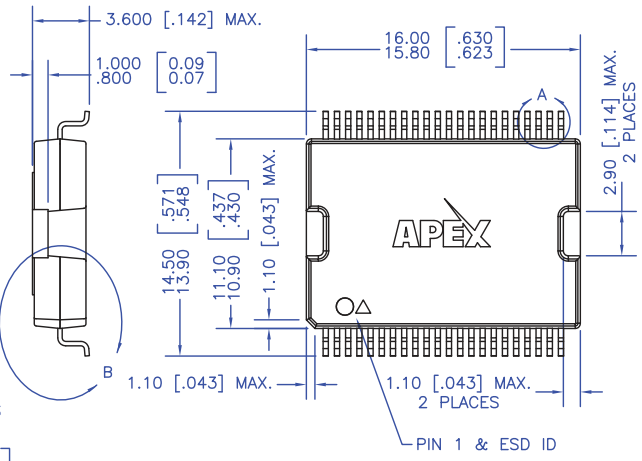
PACKAGE STYLE HU

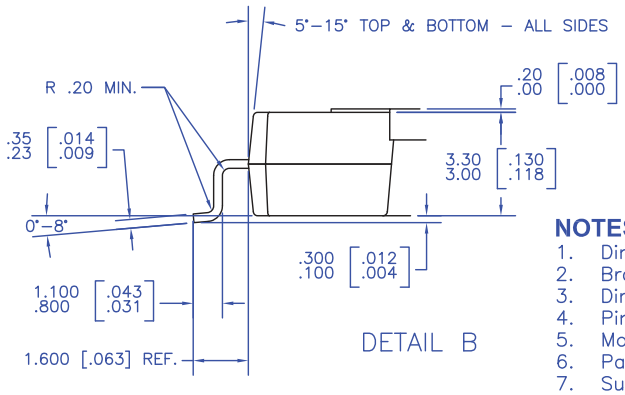






Surface Mount Layout





NOTES:

1. Dimensions are millimeters & [inches].
2. Bracketed alternate units are for reference only.
3. Dimple on lid & ESD triangle denote pin 1.
4. Pins & Heat Slug: C19400 & C10200 copper with plated finish.
5. Mold compound: Epoxy
6. Package weight: .086 oz. [2.44 g]
7. Suggested surface mount layout for reference only.