

High Voltage Power Operational Amplifiers



FEATURES

- High Voltage — 450V ($\pm 225V$)
- High Slew Rate μs
- High Output Current m
- 2MHz Power Bandwidth

APPLICATIONS

- High Voltage Instrumentation
- Piezo Transducer Excitation
- Programmable Power Supplies Up To 430V
- Electrostatic Transducers & Deflection

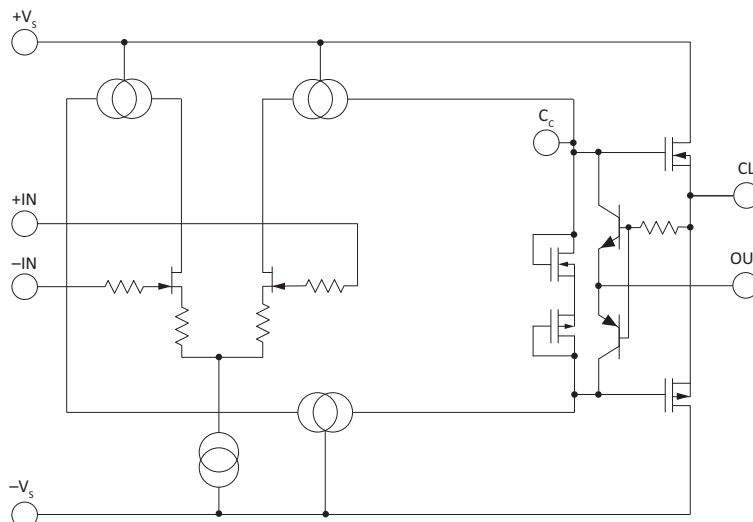


DESCRIPTION

The PA198 is a 450V high-power operational amplifier. This high voltage amplifier utilizes a MOSFET output stage and has a power bandwidth of up to 2MHz. When operating within a safe operating area, the PA198 has a maximum continuous current of 200mA. Output voltages can swing up to $\pm 215V$ with a dual supply and up to +440 volts with a single supply. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor.

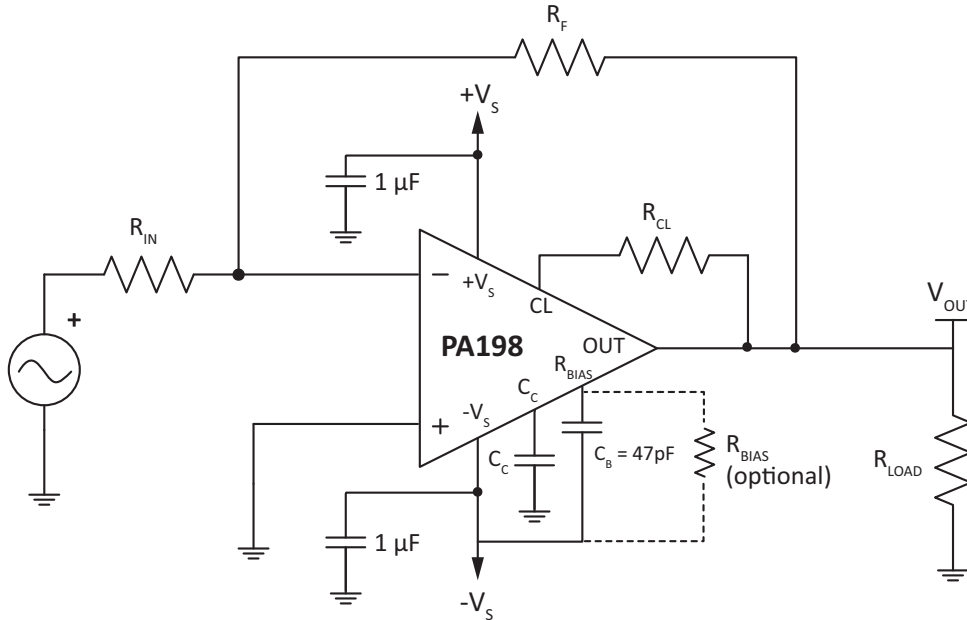
High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a bootstrapped zener-MOSFET current source. As a result, the PA198 features an unprecedented supply range and excellent supply rejection. The MOSFET output stage is biased on for linear operation. External compensation provides user flexibility. This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and silicon semiconductors. This process is used to maximize reliability, minimize size and provide exceptional performance. Ultrasonically bonded aluminum wires provide reliable interconnections over the full temperature range of the device. The Power SIP internal circuitry is electrically isolated from the heat tab.

Figure 1: Equivalent Schematic



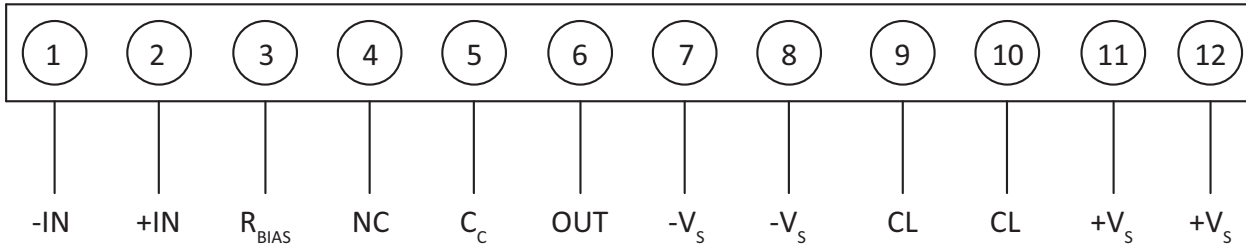
TYPICAL CONNECTIONS

Figure 2: Typical Connections



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	-IN	Inverting input.
2	+IN	Non-inverting input.
3	R _{BIAS}	Connect 47pF capacitor from this pin to -V _S pin. Optional resistor connection for quiescent current increase.
4	NC	This is a no connect, leave this pin floating.
5	C _C	Compensation Capacitive connection, select value based on Phase Compensation. See applicable section.
6	OUT	Connect pin to load and feedback resistors.
7, 8	-V _S	The negative supply rail. Pins 7 and 8 are internally connected.
9, 10	CL	Connect to the current limit resistor, and then the OUT pin. Output current flows into/out of these pins through R _{CL} . Pins 9 and 10 are internally connected.
11, 12	+V _S	The positive supply rail. Pins 11 and 12 are internally connected.

SPECIFICATIONS

Unless otherwise noted: $T_C = 25^\circ\text{C}$, compensation: $C_C = 68\text{pF}$. DC input specifications are \pm value given. Power supply voltage is typical rating.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply Voltage, total	$+V_S$ to $-V_S$		450	V
Output Current, Continuous Within SOA	I_{OUT}		200	mA
Power Dissipation, Continuous @ $T_C = 25^\circ\text{C}$ ¹	P_D		30	W
Input Voltage, Differential	$V_{IN(diff)}$	-25	+25	V
Input Voltage, Common Mode	V_{CM}	$-V_S$	$+V_S$	V
Temperature, Pin Solder, 10s max.			260	$^\circ\text{C}$
Temperature, Junction ¹	T_J		150	$^\circ\text{C}$
Temperature Range, Storage		-55	+125	$^\circ\text{C}$
Operating Temperature Range, Case	T_C	-40	+85	$^\circ\text{C}$

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. Ratings apply only to output transistors. An additional 10W may be dissipated due to quiescent power.

CAUTION

The PA198 is constructed from MOSFET transistors. ESD handling procedures must be observed. The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush machine or subject to temperatures in excess of 850°C to avoid toxic fumes.

INPUT

Parameter	Test Conditions	PA198			PA198A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, Initial			0.5	5		0.25	0.75	mV
Offset Voltage vs. Temperature	Full temp range		45			*		$\mu\text{V}/^\circ\text{C}$
Offset Voltage vs. Supply			6	10		*	*	$\mu\text{V}/\text{V}$
Offset Voltage vs. Time			75			*		$\mu\text{V}/\text{Vkh}$
Bias Current, Initial ¹			5	50		3	10	μA
Bias Current, vs. Supply			0.01			*		$\mu\text{A}/\text{V}$
Offset Current, Initial ¹			10	100		3	30	μA
Input Impedance, Dc			10^{11}			*		Ω
Input Capacitance			4			*		pF
Common Mode Voltage Range ²		$\pm V_S - 15$			*			V
Common Mode Rejection, Dc	$V_{CM} = \pm 300\text{V}$	90	110		*	*		dB
Noise	@1MHz		3			*		nV/ $\sqrt{\text{Hz}}$

1. Doubles for every 10°C of temperature increase.
2. +V_S and -V_S denote the positive and negative power supply rail respectively.

GAIN

Parameter	Test Conditions	PA198			PA198A			Units
		Min	Typ	Max	Min	Typ	Min	
Open Loop Gain @ 15 Hz		96	108		*	*		dB
Gain Bandwidth Product @ 1 MHz	R _L = Open, C _C = Open		394			*		MHz
Power Bandwidth	C _C = 12pf		1			*		MHz
	C _C = 3.3pf		1.5			*		MHz

OUTPUT

Parameter	Test Conditions	PA198			PA198A			Units
		Min	Typ	Max	Min	Type	Min	
Voltage Swing ¹	I _{OUT} = $\pm 200\text{mA}$	$\pm V_S - 10$	$\pm V_S - 6.5$		*	*		V
Current, Continuous	T _C = 85°C	± 200			*			mA
Slew Rate, A _V = 40	C _C = 12pF		1000			*		V/ μs
Slew Rate, A _V = 100	C _C = Open		2000		700			V/ μs
Capacitive Load, A _V = +1	Full temp range	470			*			pF
Settling Time to 0.1%, A _V = -100	C _C = Open, 2V step		750			*		ns

Resistance, No Load	$R_{CL} = 0$		50			*		Ω
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1. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.

POWER SUPPLY

Parameter	Test Conditions	PA198			PA198A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage ¹	Full temp range	± 15	± 150	± 225	*	*	*	V
Current, quiescent			22.5	25		*	*	mA
Current, quiescent with $R_{BIAS}=5k\Omega$			25.3			*		mA
Current, quiescent vs. temperature			5.2			*		$\mu A/^\circ C$
Current, quiescent vs. supply			0.8			*		$\mu A/V$

1. Derate max supply rating 0.625 V/ $^\circ C$ below 25 $^\circ C$ case temperature. No derating needed above 25 $^\circ C$ case.

THERMAL

Parameter	Test Conditions	PA198			PA198A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, Ac, Junction To Case ¹	Full temp range, $F > 60$ Hz			2.5			*	$^\circ C/W$
Resistance, Dc, Junction To Case	Full temp range, $F < 60$ Hz			4.2			*	$^\circ C/W$
Resistance, Junction To Air	Full temp range		30			*		$^\circ C/W$
Temperature Range, Case	Meets full range specifications	-25		+85	*		*	$^\circ C$

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

Note: *The specification of PA198A is identical to the specification for PA198 in applicable column to the left.

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

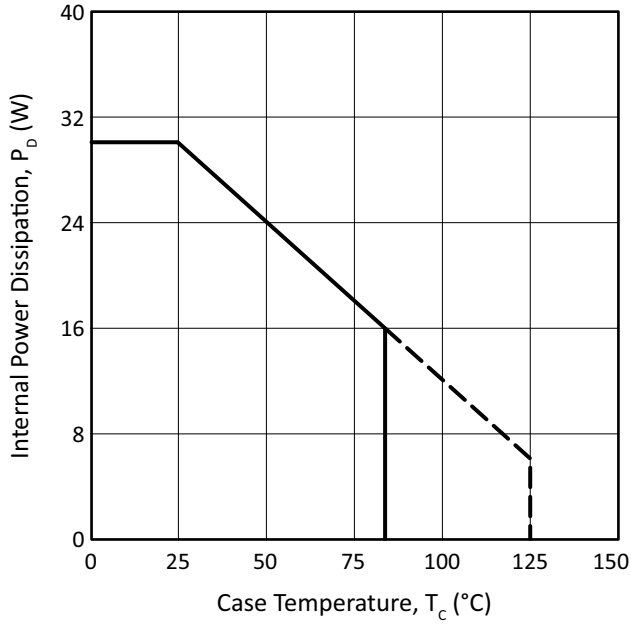


Figure 5: Quiescent Current

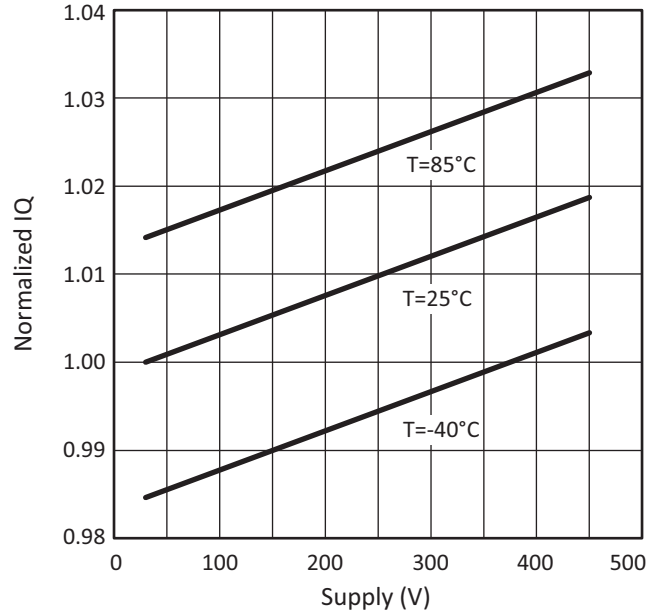


Figure 6: Small Signal Response

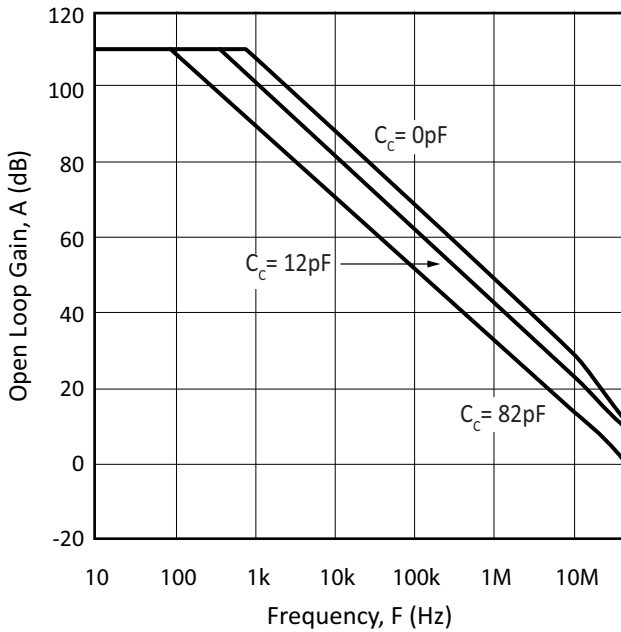


Figure 7: Phase Response

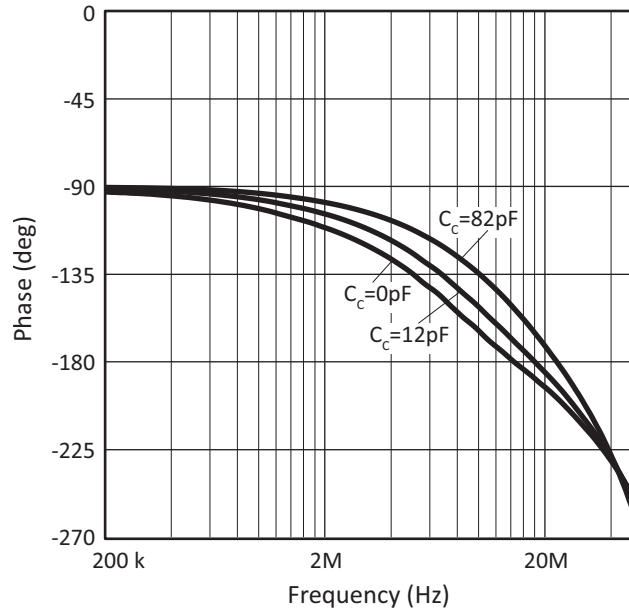


Figure 8: Output Voltage Swing

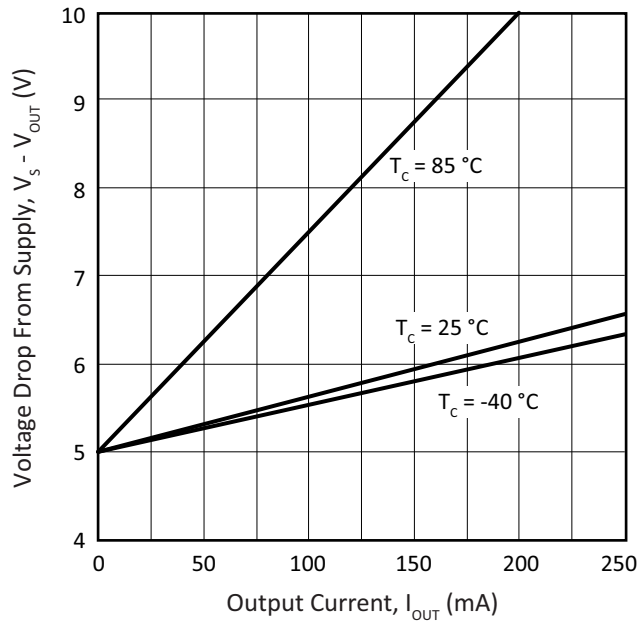


Figure 9: Power Response

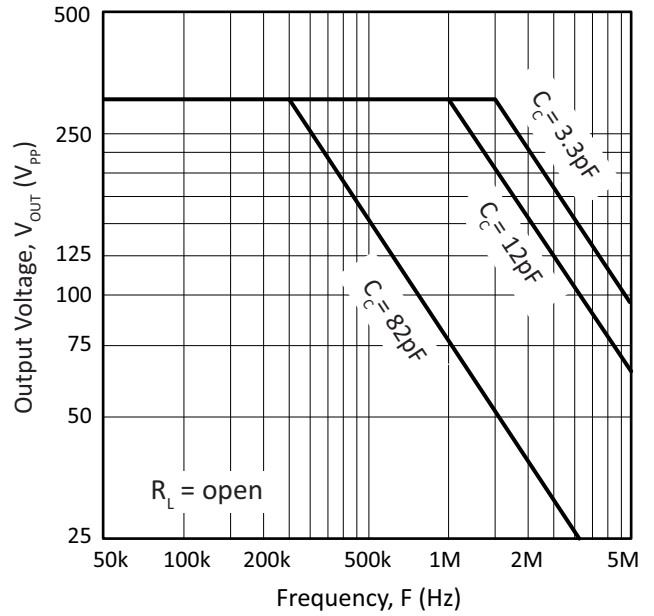


Figure 10: Slew Rate

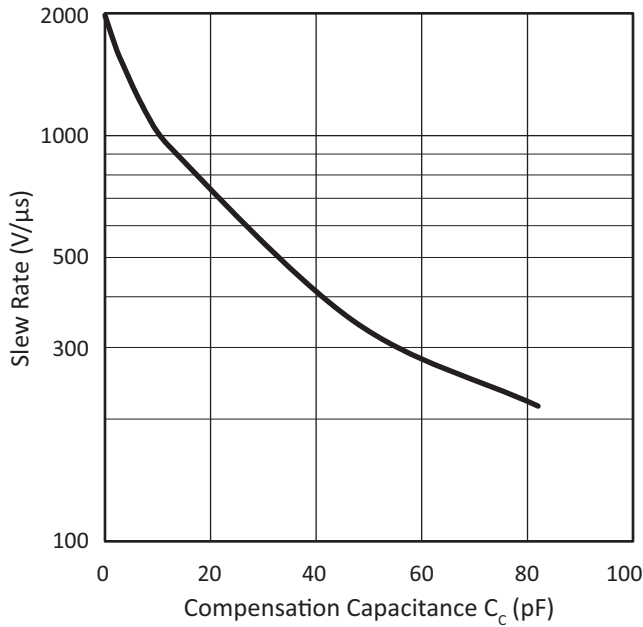


Figure 11: Harmonic Distortion

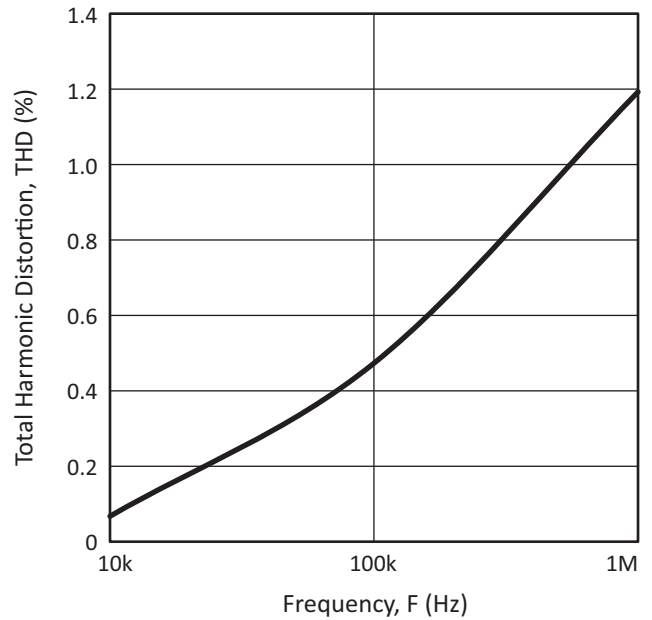


Figure 12: Input Noise Voltage

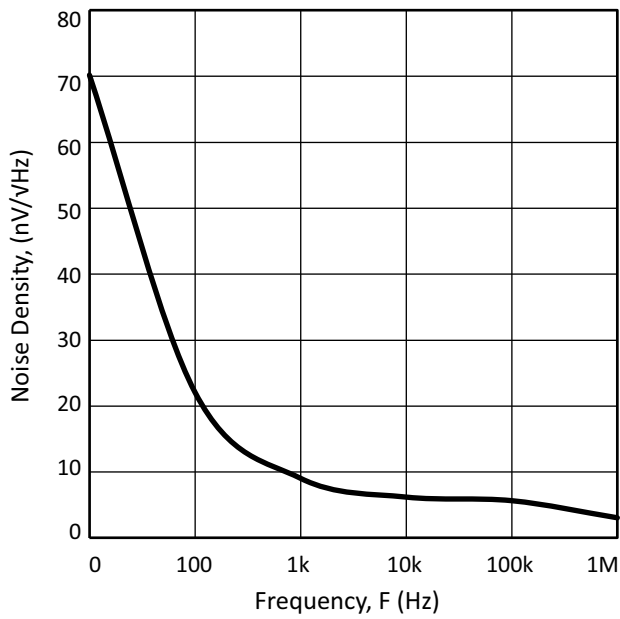


Figure 13: Common Mode Rejection

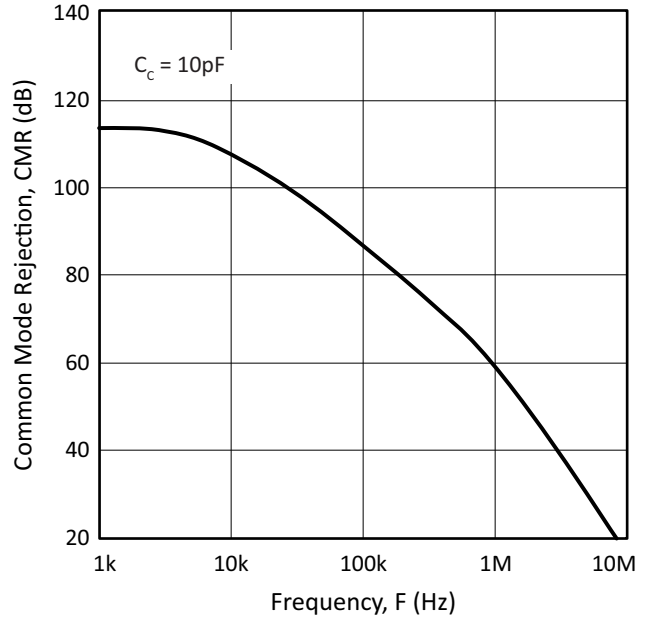


Figure 14: Power Supply Rejection

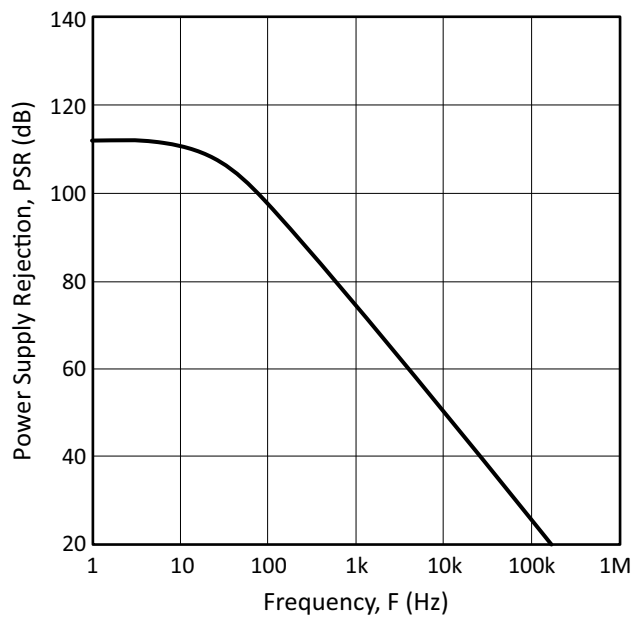


Figure 15: Current Limit

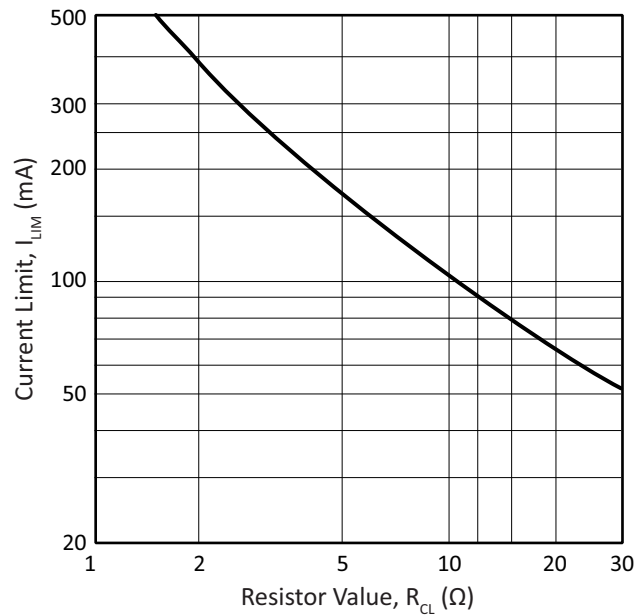


Figure 16: Quiescent Current vs R_{BIAS}

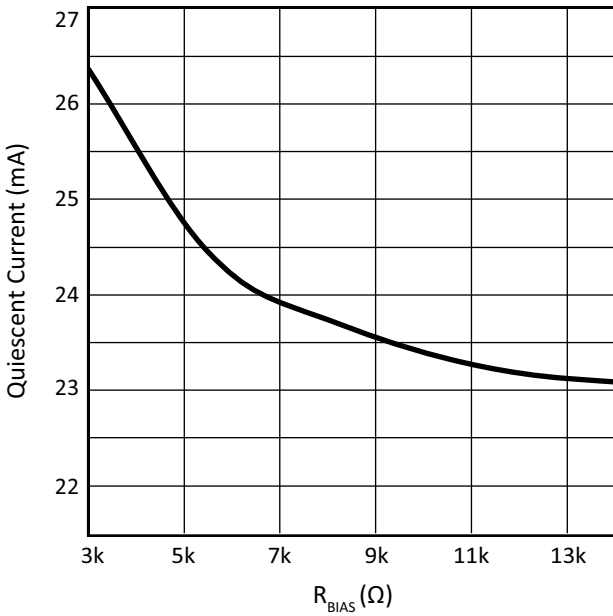


Figure 17: Slew Rate vs R_{BIAS}

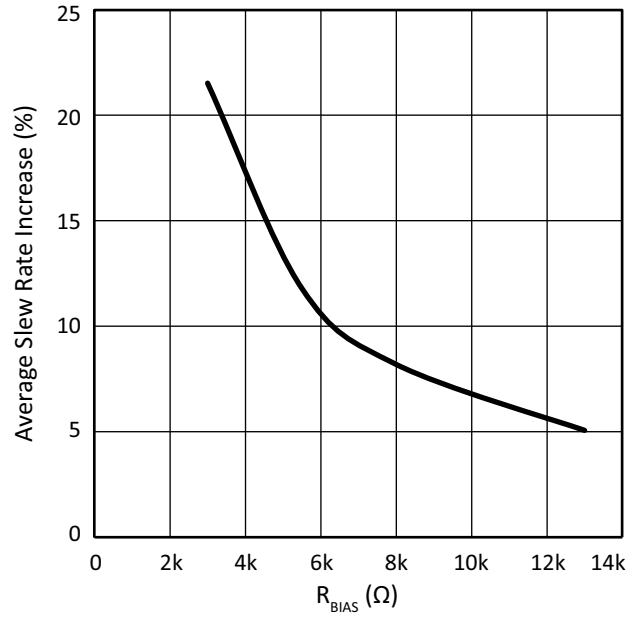


Figure 18: Pulse Response

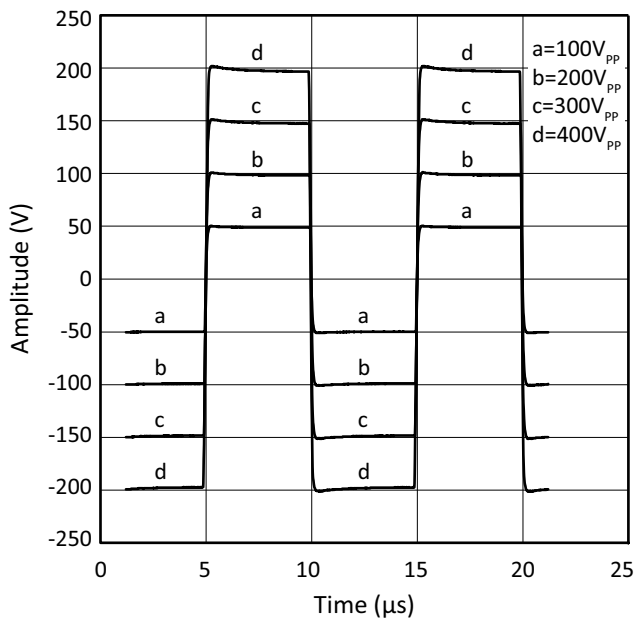
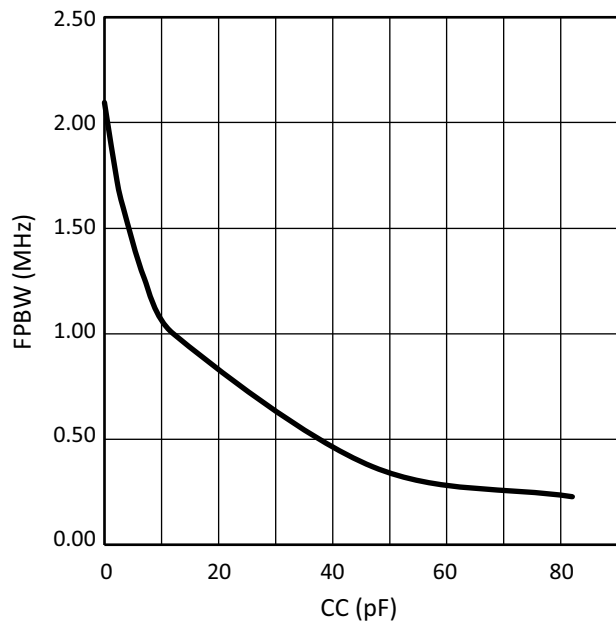


Figure 19: Full Power Bandwidth vs CC



SAFE OPERATING AREA (SOA)

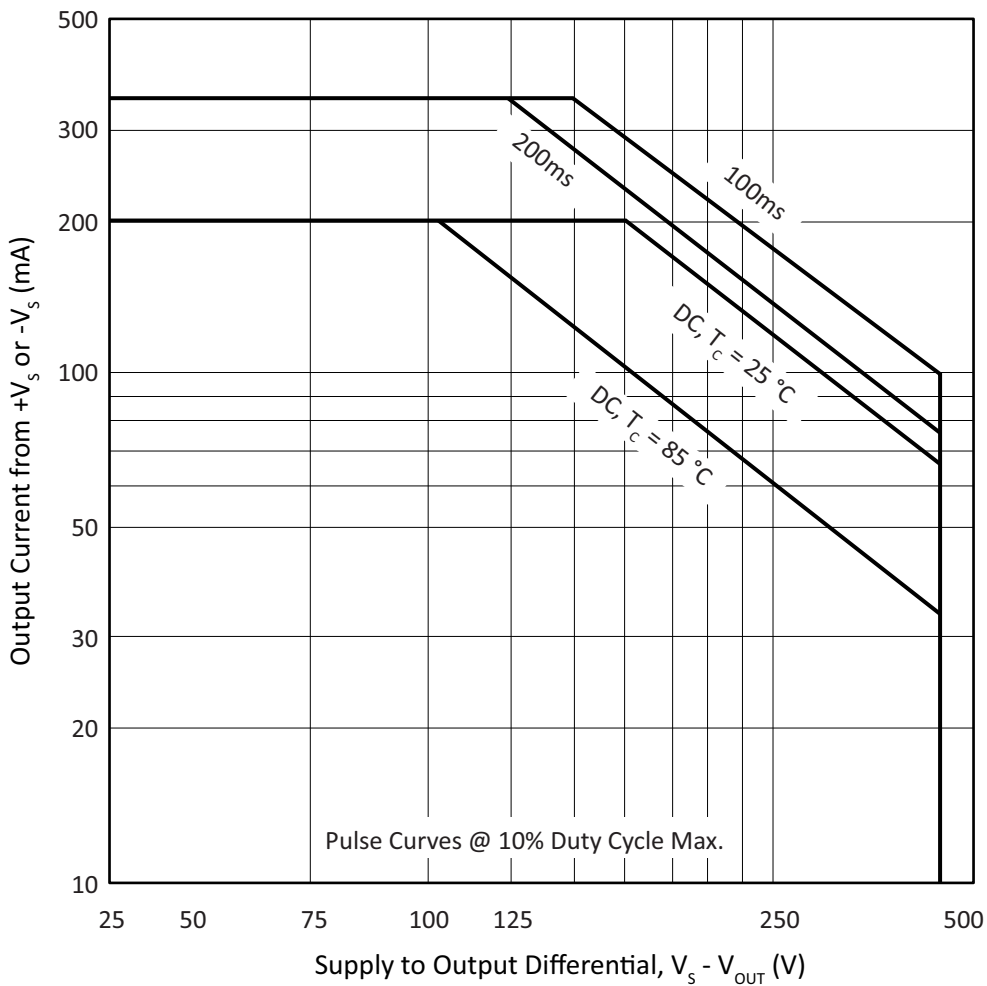
The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

Note: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

Figure 20: SOA



GENERAL

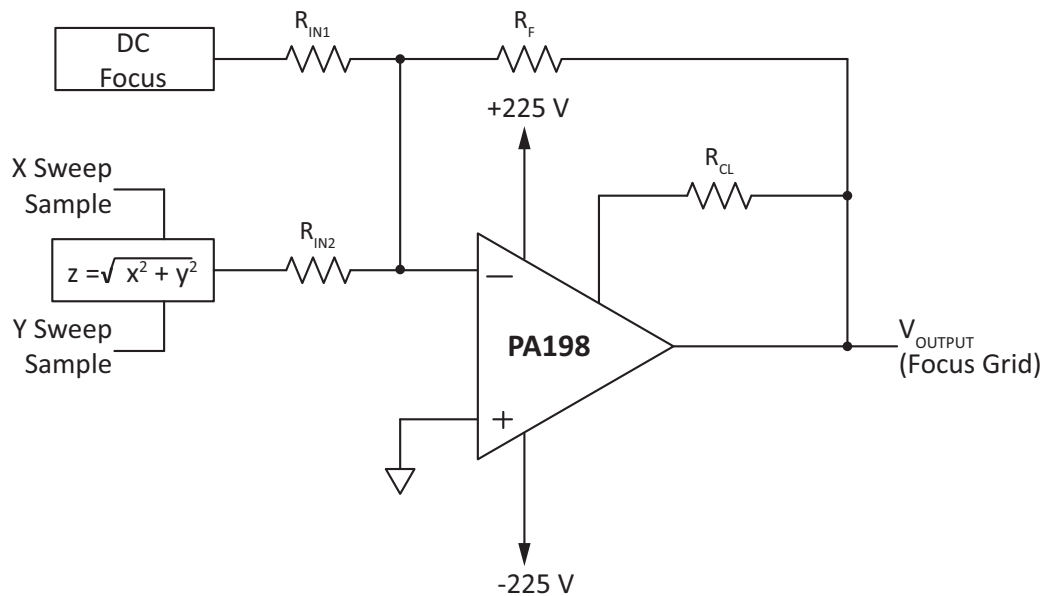
Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

DYNAMIC FOCUSING

Dynamic focusing is the active correction of focusing voltage as a beam traverses the face of a CRT. This is necessary in high resolution flat face monitors since the distance between cathode and screen varies as the beam moves from the center of the screen to the edges. PA198 lends itself well to this function since it can be connected as a summing amplifier with inputs from the nominal focus potential and the dynamic correction. The nominal might be derived from a potentiometer, or perhaps automatic focusing circuitry might be used to generate this potential. The dynamic correction is generated from the sweep voltages, by calculating the distance of the beam from the center of the display.

Figure 21: Typical Application



PHASE COMPENSATION

Gain	C _C
1	270pF
40	12pF
100	open

C_C Rated For Full Supply Voltage

R BIAS

The RBIAS feature of the PA198 allows the user to increase slew rate by way of increasing quiescent current with a resistance from Pin 3(RBIAS) to Pin 7(-Vs). The possible values of resistance and effects of this feature are characterized in figures 16 and 17. In all cases, whether the feature is being used or not, there should be a 47pF capacitance connected from Pin3 to Pin7 to ensure stability.

CURRENT LIMIT

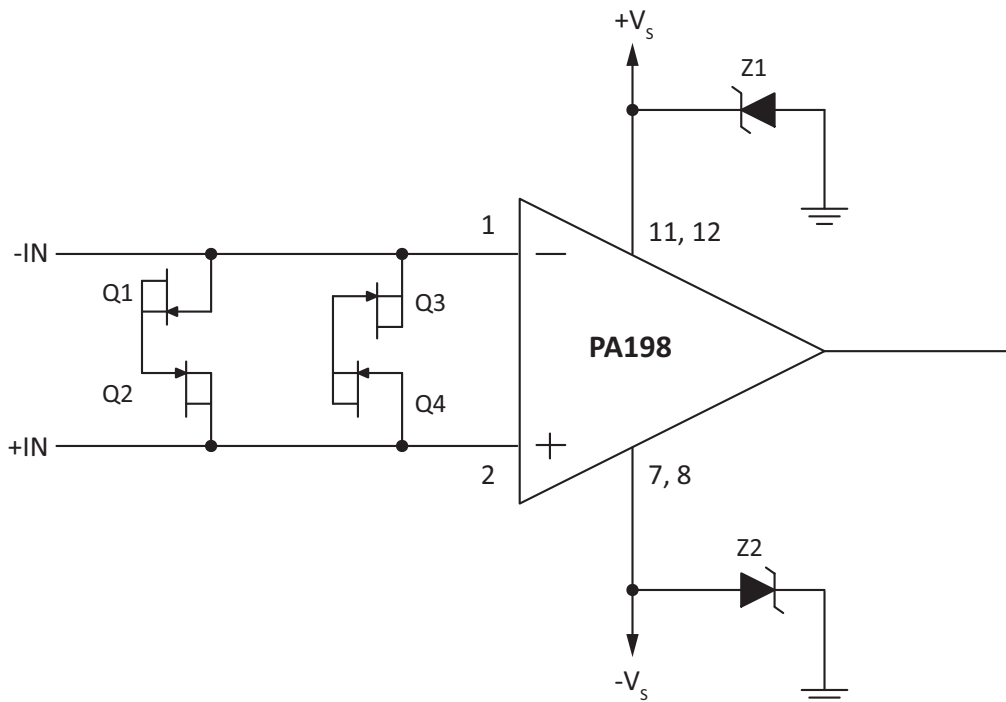
For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the typical connection diagram. The minimum value is 3.1 Ω , however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30 ohms.

$$R_{CL}(\Omega) = \frac{0.7V}{I_{CL} - 0.03(A)}$$

INPUT PROTECTION

Although the PA198 can withstand differential voltages up to $\pm 25V$, additional external protection is recommended. Since the PA198 is a high speed amplifier, low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 17). The differential input voltage will be clamped to $\pm 1.4V$. This is sufficient overdrive to produce maximum power bandwidth.

Figure 22: Overvoltage Protection



POWER SUPPLY PROTECTION

Unidirectional transient voltage suppressors diodes are recommended as protection on the supply pins. The diodes clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the diodes are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail are known to induce input stage failure. Unidirectional TVS diodes prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

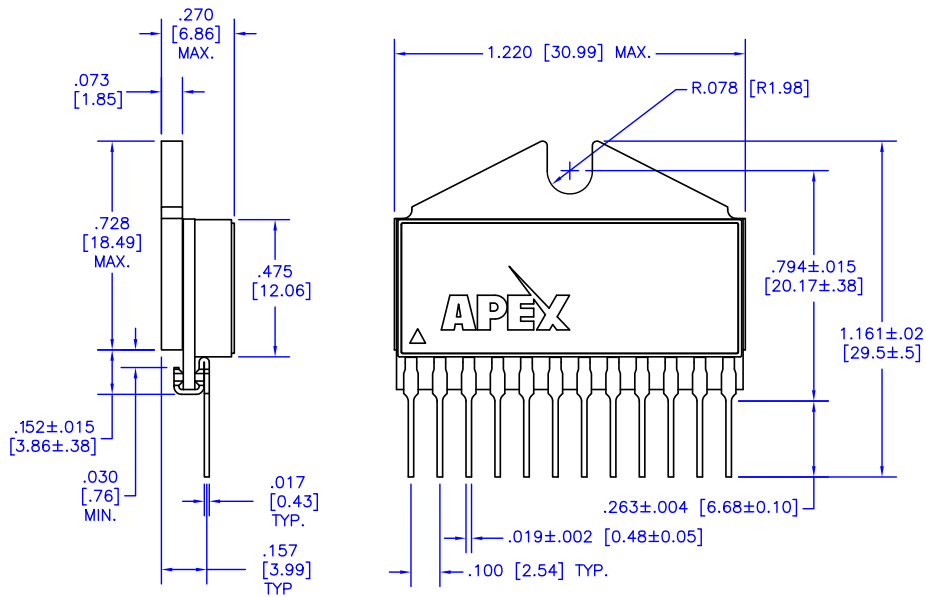
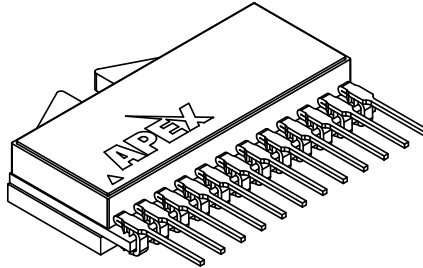
STABILITY

The PA198 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_C must be mounted closely to the amplifier pins 7 and 8 to avoid spurious oscillation.

PACKAGE OPTIONS

Part Number	Apex Package Style	Description
PA198DP	DP	12-Pin SIP
PA198EE	EE	12-Pin SIP w/90° formed leads, tab up
PA198FP	FP	12-Pin SIP w/90° formed leads, tab down

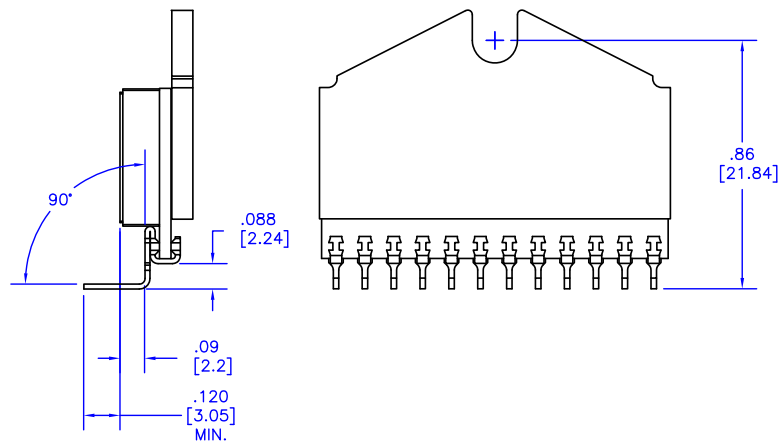
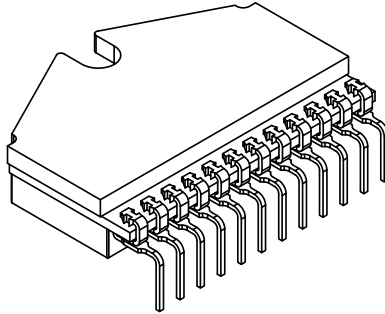
PACKAGE STYLE DP



NOTES:

1. Dimensions are inches & [mm].
2. Triangle on lid denotes pin 1.
3. Pins: Alloy 510 phosphor bronze plated with matte tin (150 – 300µ") over nickel (50 µ" max.) underplate.
4. Package: Vectra liquid crystal polymer, black
5. Epoxy-sealed & ultrasonically welded non-hermetic package.
6. Package weight: .367 oz. [11.41 g]

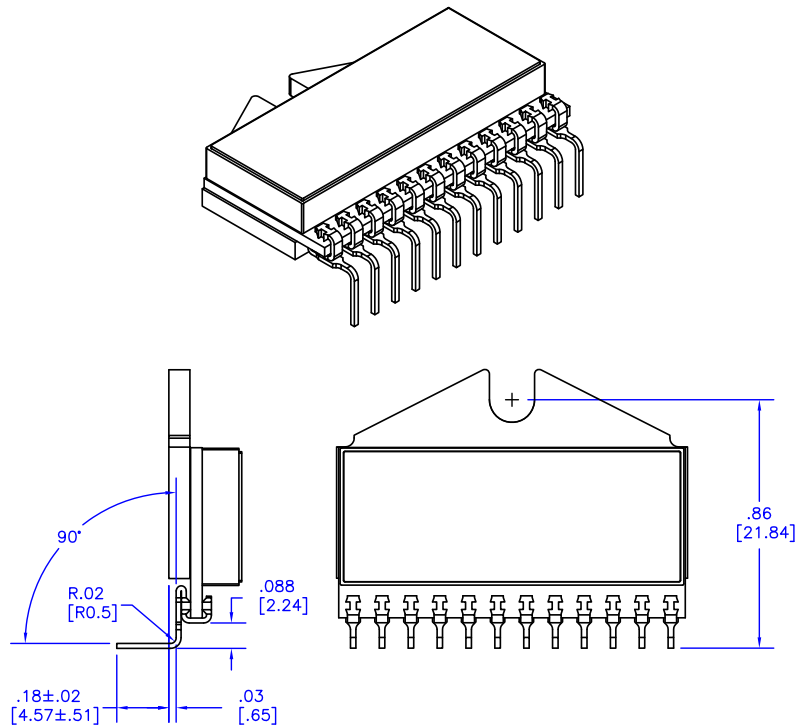
PACKAGE STYLE EE



NOTES:

1. Dimensions are inches & [mm].
2. For other dimensions and information on this package with unformed leads, see package DP.

PACKAGE STYLE FP



NOTES:

1. Dimensions are inches & [mm].
2. For other dimensions and information on this package with unformed leads, see package DP.

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