PA12R

Radiation Tolerant Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- Low Thermal Resistance — 1.4°C/W
- Wide Supply Range — ±10V to ±50V
- High Output Current — Up to ±15A Peak
- Single Event Effect (SEE) Testing - 62.5 MeV.cm^2/mg
- Total Ionizing Dose (TID) Testing - 50krad (Si)

APPLICATIONS

- Motor, Valve, and Actuator Control
- Magnetic Deflection Circuits up to 10A
- Power Transducers up to 100 kHz
- Programmable Power Supplies up to 90V
- Fine Steering and Deformable Mirrors
- Voice Coils and Solenoids

DESCRIPTION

The PA12R is a state of the art high voltage, very high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. For continuous operation under load, a heatsink of proper rating is recommended. The PA12R is not recommended for gains below –3 (inverting) or +4 (non-inverting).

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

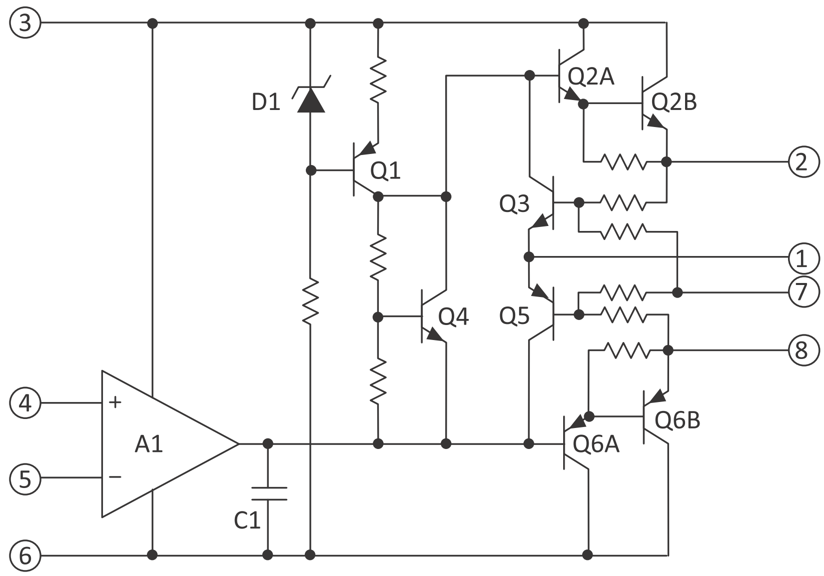
APEX RAD TOLERANT OVERVIEW

As an Apex radiation tolerant device, PA12R has been tested to “M/883” compliance. Additional testing for radiation tolerance includes:

- Particle Impact Noise Detection (PIND) Testing
- Single Event Effect (SEE) Testing: 62.5 MeV.cm^2/mg, Xenon heavy ion
- Enhanced Low Dose Rate Sensitivity (ELDRS) Testing: Dosage: 50 krad (Si)
- High-Dosage Radiation (HDR) Testing: Dosage: 50 krad (Si)

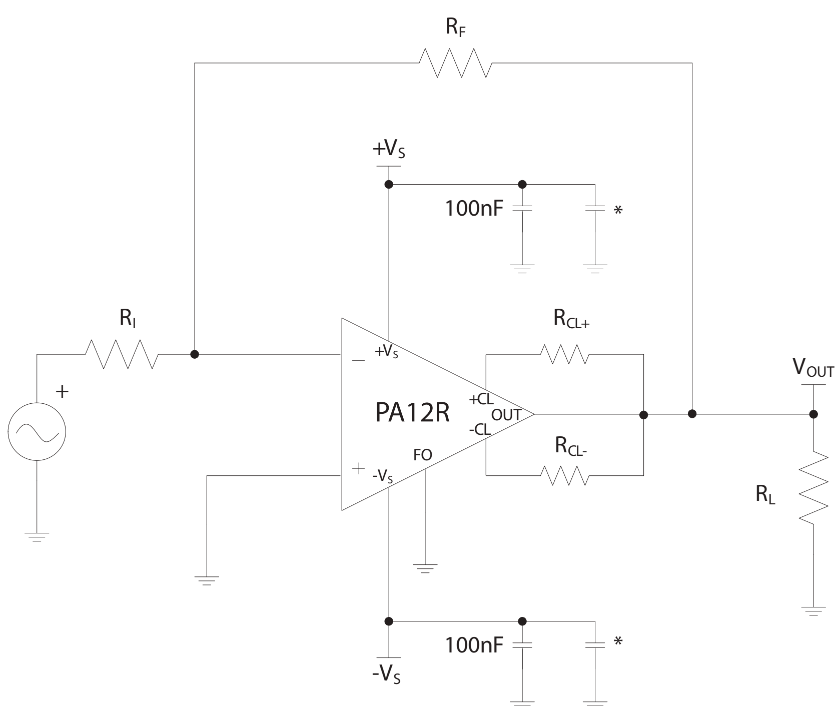
Apex radiation tolerant devices are considered “Class-H”, or radiation-tolerant. These devices do not satisfy the requirements for “Class-K” or radiation-hardened devices.

Figure 1: Equivalent Schematic



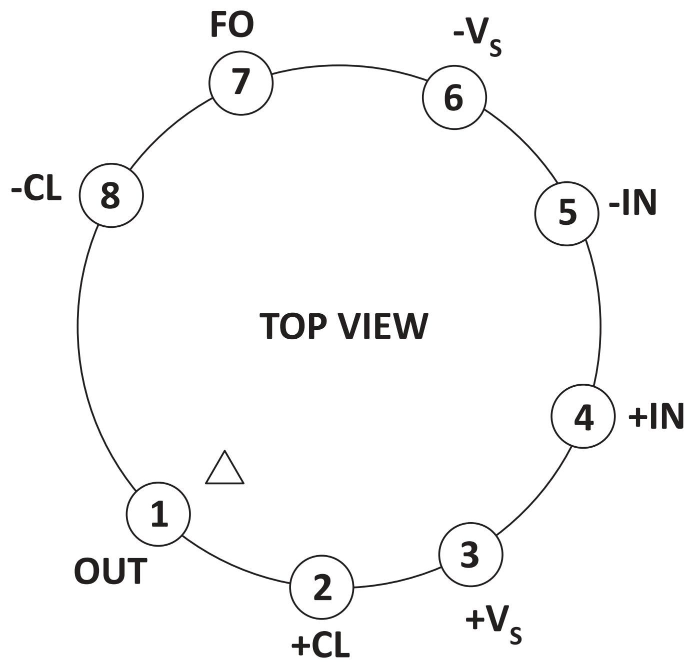
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	OUT	The output. Connect this pin to load and to the feedback resistors.
2	+CL	Connect to the sourcing current limit resistor, and then the OUT pin. Output current flows out of this pin through R_{CL+}.
3	+Vs	The positive supply rail.
4	+IN	The non-inverting input.
5	-IN	The inverting input.
6	-Vs	The negative supply rail.
7	FO	The foldover current limit. Connect to ground if desired. See 'Current Limiting' section.
8	-CL	Connect to the sinking current limit resistor, and then the OUT pin. Output current flows into this pin through R_{CL-}.

SPECIFICATIONS

Unless otherwise noted: The power supply voltage for all tests is ±40. Full temperature range specifications are guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, +Vs to –Vs	$+V_S$ to $-V_S$		100	V
Output Current, within SOA	I_O		15	A
Power Dissipation, internal	P_D		125	W
Input Voltage, differential	$V_{IN\ (Diff)}$		±37	V
Input Voltage, common mode	V_{cm}		$\pm V_S$	V
Temperature, pin solder 10s			350	°C
Temperature, junction [1]	T_J		200	°C
Temperature Range, storage		-65	+150	°C
Operating Temperature Range, case	T_C	-55	+125	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess to 850°C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	PA12			PA12R			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial[2]	T_C = 25°C		±2	±6		±1		mV
Offset Voltage vs. temperature	Full temp range		±10	±65		*	*	μV/°C
Offset Voltage vs. supply	T_C = 25°C		±30	±200		*	*	μV/V
Offset Voltage vs. power	T_C = 25°C		±20			*		μV/W
Bias Current, initial[2]	T_C = 25°C		±12	±30		9		nA
Bias Current vs. temperature	Full temp range		±50	±500		*	*	pA/°C
Bias Current vs. supply	T_C = 25°C		±10			*		pA/V
Offset Current, initial[2]	T_C = 25°C		±12	±30		4		nA
Offset Current vs. temperature	Full temp range		±50			*		pA/°C
Input Impedance, DC	T_C = 25°C		200			*		MΩ
Input Capacitance	T_C = 25°C		3			*		pF
Common Mode Voltage Range [1]	Full temp range	$\pm V_S -5$	$\pm V_S -3$					V
Common Mode Rejection, DC[2]	Full temp range, $V_{CM} = \pm V_S -6V$	74	100			99		dB

1. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
2. Typical values are based on a sample of PA12Rs that underwent radiation testing, reflecting the average of the biased and unbiased HDR data at 50krad. These values provide a general overview of performance; however, the full PA12R Radiation Report should be consulted prior to flight.

GAIN

Parameter	Test Conditions	PA12			PA12R			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop Gain @ 10 Hz	T_C = 25°C, 1 kΩ load		110			*		dB
Open Loop Gain @ 10 Hz[1]	Full temp range, 8 Ω load	96	108			103		dB
Gain Bandwidth Product @ 1 MHz	T_C = 25°C, 8 Ω load		4			*		MHz
Power Bandwidth	T_C = 25°C, 8 Ω load	13	20		*	*		kHz
Phase Margin, A_V = +4	Full temp range, 8 Ω load		20			*		°

1. Typical values are based on a sample of PA12Rs that underwent radiation testing, reflecting the average of the biased and unbiased HDR data at 50krad. These values provide a general overview of performance; however, the full PA12R Radiation Report should be consulted prior to flight.

OUTPUT

Parameter	Test Conditions	PA12 Min	PA12 Typ	PA12 Max	PA12R Min	PA12R Typ	PA12R Max	Units
Voltage Swing [1]	T_C = 25°C, PA12 = 10A, PA12A = 15A	$\pm V_S - 6$			*			V
Voltage Swing [1]	T_C = 25°C, I_O = 5A	$\pm V_S - 5$			*			V
Voltage Swing [1,2]	Full temp range, I_O = 80mA	$\pm V_S - 5$				$\pm V_S - 3$		V
Current, peak	T_C = 25°C	10			*			A
Settling Time to 0.1%	T_C=25°C, 2V step		2			*		µs
Slew Rate[2]	T_C = 25°C	2.5	4			5		V/µs
Capacitive Load	Full temp range, A_V = 4			1.5			*	nF
Capacitive Load	Full temp range, A_V > 10			SOA			*	

1. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
2. Typical values are based on a sample of PA12Rs that underwent radiation testing, reflecting the average of the biased and unbiased HDR data at 50krad. These values provide a general overview of performance; however, the full PA12R Radiation Report should be consulted prior to flight.

POWER SUPPLY

Parameter	Test Conditions	PA12 Min	PA12 Typ	PA12 Max	PA12R Min	PA12R Typ	PA12R Max	Units
Voltage	Full temp range	±10	±40	±45	*	*	*	V
Current, quiescent[1]	T_C = 25°C		25	50		22		mA

1. Typical values are based on a sample of PA12Rs that underwent radiation testing, reflecting the average of the biased and unbiased HDR data at 50krad. These values provide a general overview of performance; however, the full PA12R Radiation Report should be consulted prior to flight.

THERMAL

Parameter	Test Conditions	PA12			PA12R			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case [1]	T_C= -55 to 125°C F > 60 Hz		0.8	0.9		*	*	°C/W
Resistance, DC, junction to case	T_C= –55 to 125°C		1.25	1.4		*	*	°C/W
Resistance, junction to air	T_C= –55 to 125°C		30			*		°C/W
Temperature Range, case	Meets full range specs	-25		+85	-55		+125	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

Note: * The specifications were not measured under radiation. In a non-radiation environment, the PA12 parameters reflect the behavior of the PA12R. However, in a radiation environment, the PA12R specifications marked with an asterisk (excluding thermal specifications) are likely to deviate from the PA12 specifications.

TYPICAL PERFORMANCE GRAPHS (PA12)

Figure 4: Power Derating

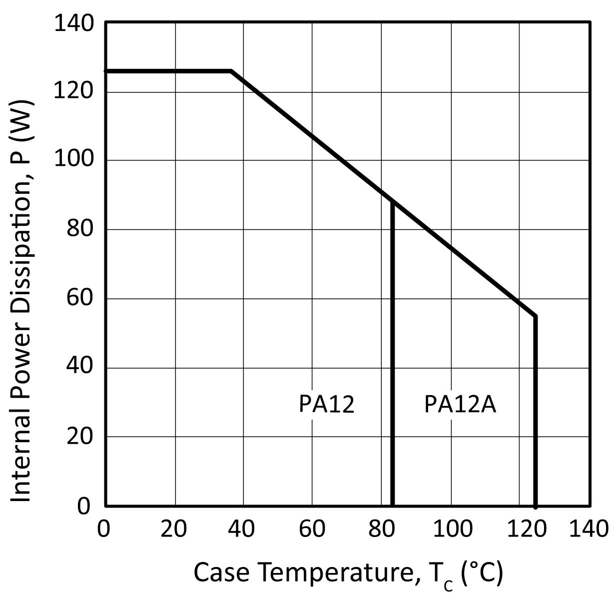


Figure 5: Bias Current vs Temperature

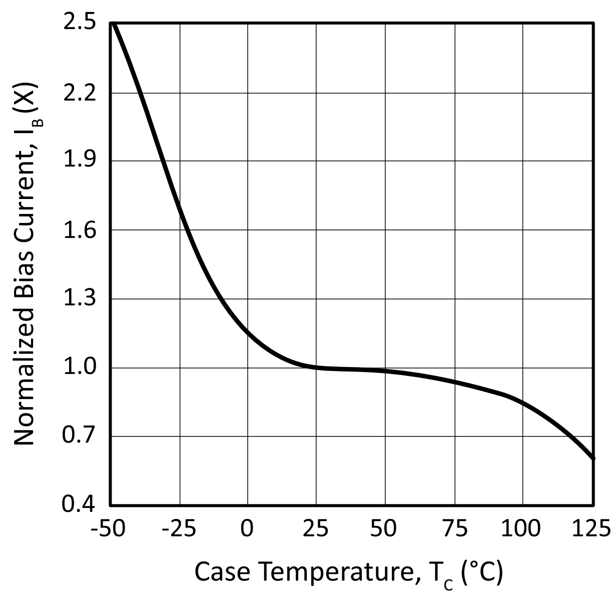


Figure 6: Small Signal Response

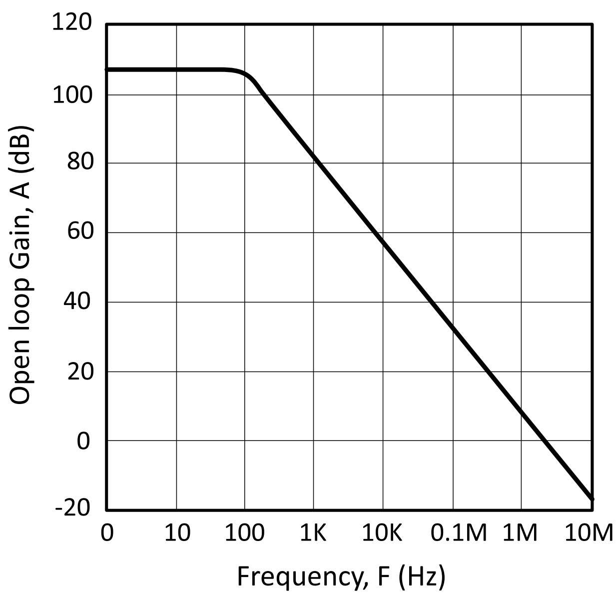


Figure 7: Phase Response

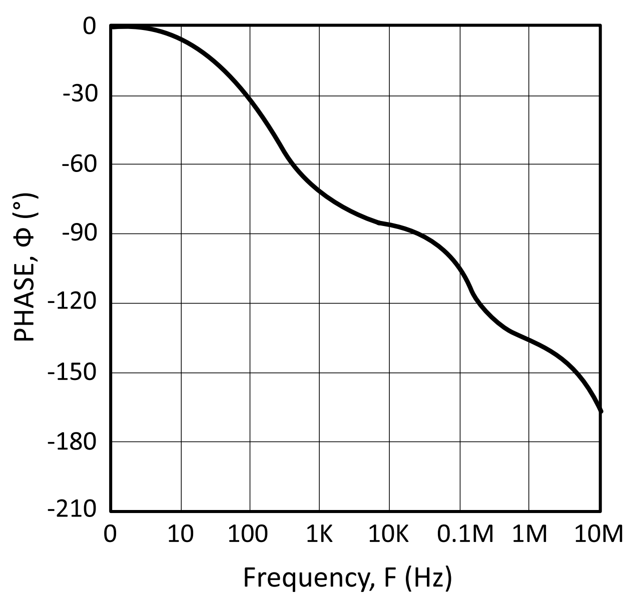


Figure 8: Current Limit vs Temperature

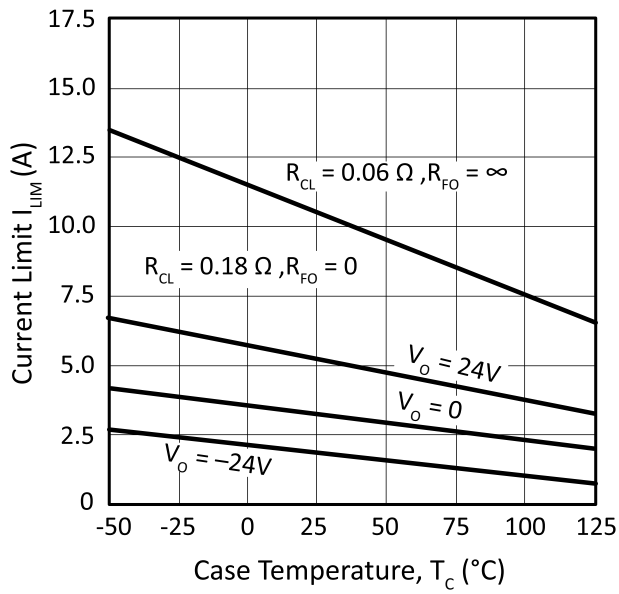


Figure 9: Power Response

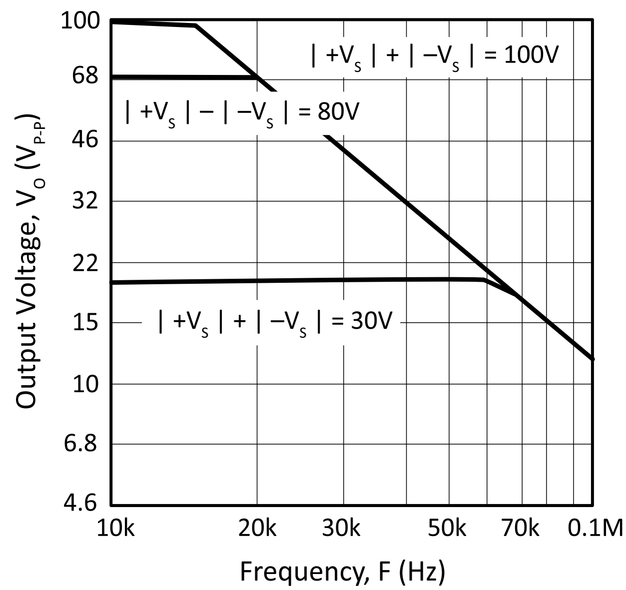


Figure 10: Common Mode Rejection

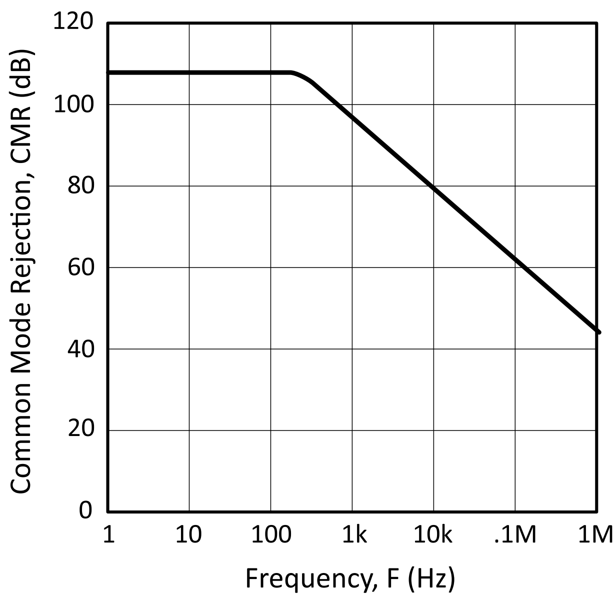


Figure 11: Pulse Response

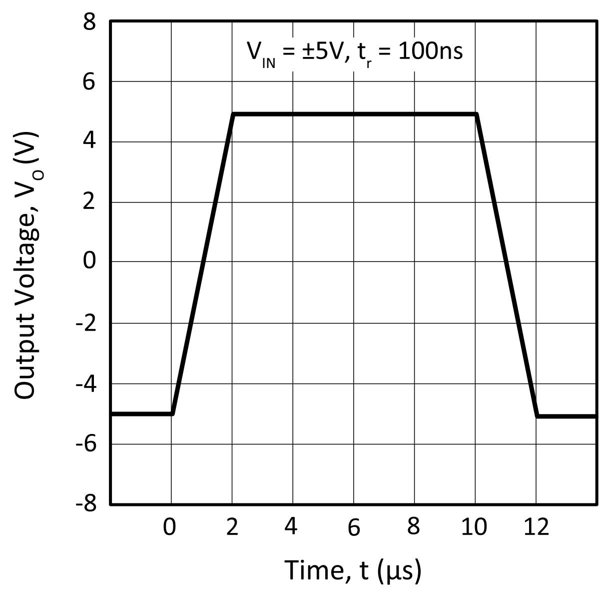


Figure 12: Input Noise

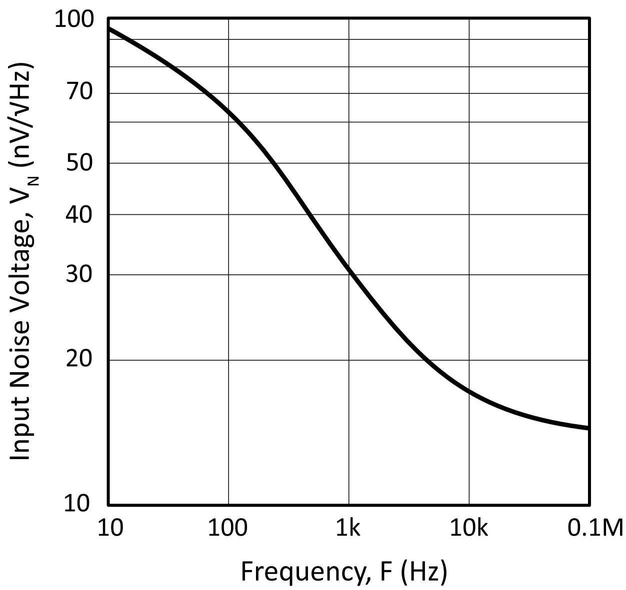


Figure 13: Harmonic Distortion

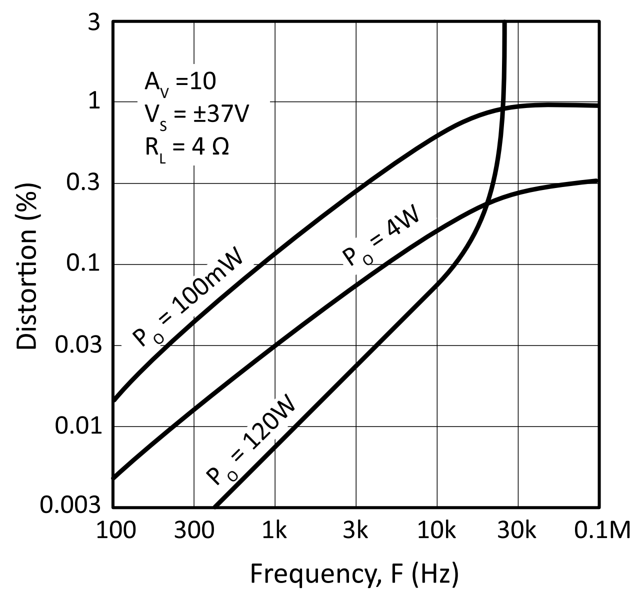


Figure 14: Quiescent Current vs V_S

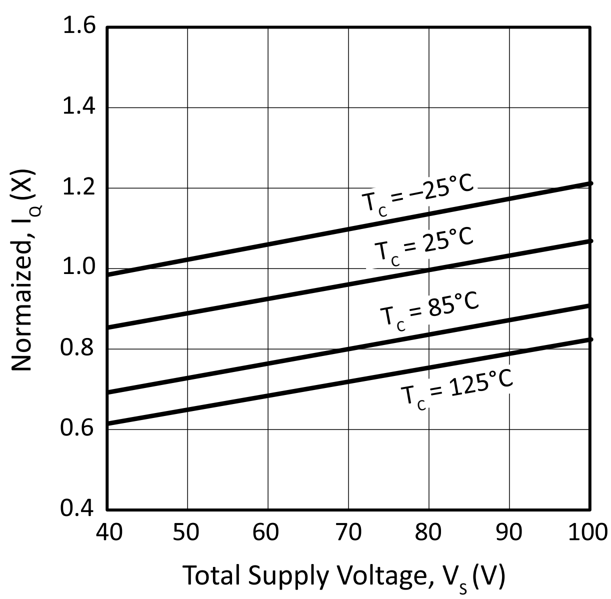
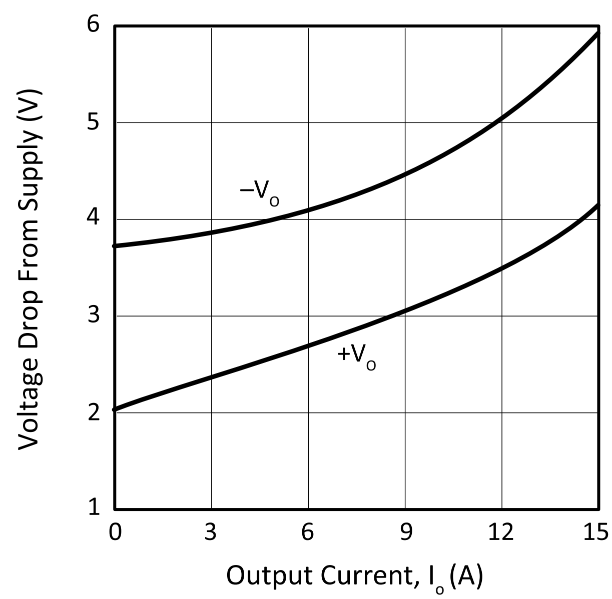


Figure 15: Output Voltage Swing

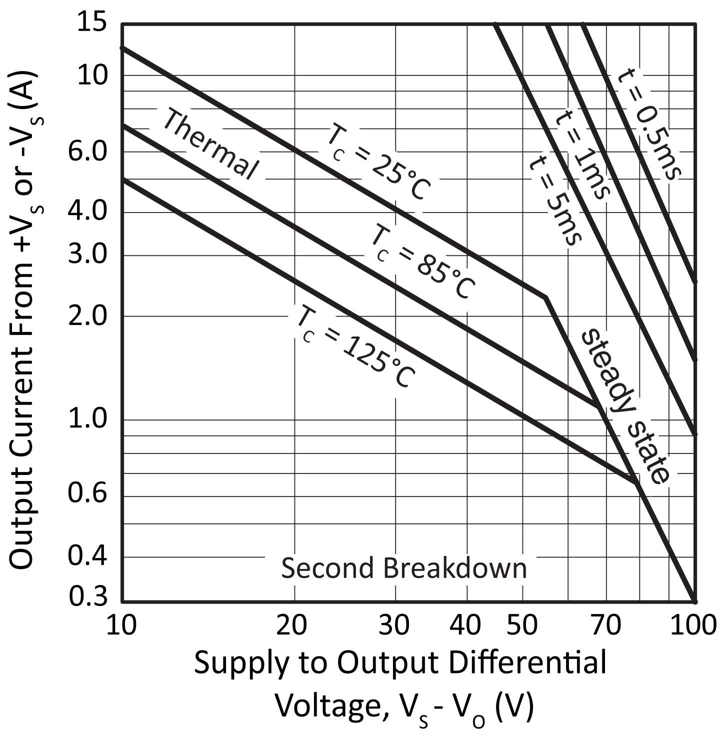


SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.

Figure 16: SOA



The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified.

±V_S	Capacitive Load		Inductive Load	
	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
50V	200µF	125µF	5m H	2.0 mH
40V	500µF	350µF	15 mH	3.0 mH
35V	2.0mF	850µF	50 mH	5.0 mH
30V	7.0mF	2.5mF	150 mH	10 mH
25V	25mF	10mF	500 mH	20 mH
20V	60mF	20mF	1,000 mH	30 mH
15V	150mF	60mF	2,500 mH	50 mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 15A or 25V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or common if the current limits are set as follows at T_C = 25°C:

±V_S	**Short to ±V_S C, L, or EMF Load**	**Short to Common**
50V	0.30A	2.4A
40V	0.58A	2.9A
35V	0.87A	3.7A
30V	1.5A	4.1A
25V	2.4A	4.9A
20V	2.9A	6.3A
15V	4.2A	8.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

POWER RATING

Not all vendors use the same method to rate the power handling capability of a Power Op Amp. Apex Microtechnology rates the internal dissipation, which is consistent with rating methods used by transistor manufacturers and gives conservative results. Rating delivered power is highly application dependent and therefore can be misleading. For example, the 125W internal dissipation rating of the PA12R could be expressed as an output rating of 250W for audio (sine wave) or as 440W if using a single ended DC load. Please note that all vendors rate maximum power using an infinite heatsink.

THERMAL STABILITY

Apex Microtechnology has eliminated the tendency of class A/B output stages toward thermal runaway and thus has vastly increased amplifier reliability. This feature, not found in most other Power Op Amps, was pioneered by Apex Microtechnology in 1981 using thermistors which assure a negative temperature coefficient in the quiescent current. The reliability benefits of this added circuitry far outweigh the slight increase in component count.

CURRENT LIMITING

Refer to Application Note 9, “Current Limiting”, for details of both fixed and fold over current limit operation. Beware that current limit should be thought of as a +/–20% function initially and varies about 2:1 over the range of –55°C to 125°C.

For fixed current limit, leave pin 7 open and use equations 1 and 2.

1.

$$R_{CL}(\Omega) = \frac{0.65V}{I_{CL}(A)}$$

2.

$$I_{CL}(A) = \frac{0.65V}{R_{CL}(\Omega)}$$

Where:

- I_{CL} is the current limit in amperes.
- R_{CL} is the current limit resistor in ohms.

For certain applications, fold over current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum fold over slope, ground pin 7 and use equations 3 and 4.

3.

$$I_{CL}(A) = \frac{0.65V + (Vo \cdot 0.014)}{R_{CL}(\Omega)}$$

4.

$$R_{CL}(\Omega) = \frac{0.65V + (Vo \cdot 0.014)}{I_{CL}(A)}$$

Where:

- Vo is the output voltage in volts.

Most designers start with either equation 1 to set R_{CL} for the desired current at 0V out, or with equation 4 to set R_{CL} at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor (R_{FO}) between pin 7 and ground. Use equations 5 and 6 with this new resistor in the circuit.

5.

$$I_{CL}(A) = \frac{0.65V + \dfrac{Vo \cdot 0.14}{10.14 + R_{FO}(k\Omega)}}{R_{CL}(\Omega)}$$

6.

$$R_{CL}(\Omega) = \frac{0.65V + \dfrac{Vo \cdot 0.14}{10.14 + R_{FO}(k\Omega)}}{I_{CL}(A)}$$

Where:

- R_{FO} is in K ohms.

TABLE 4 GROUP A INSPECTION

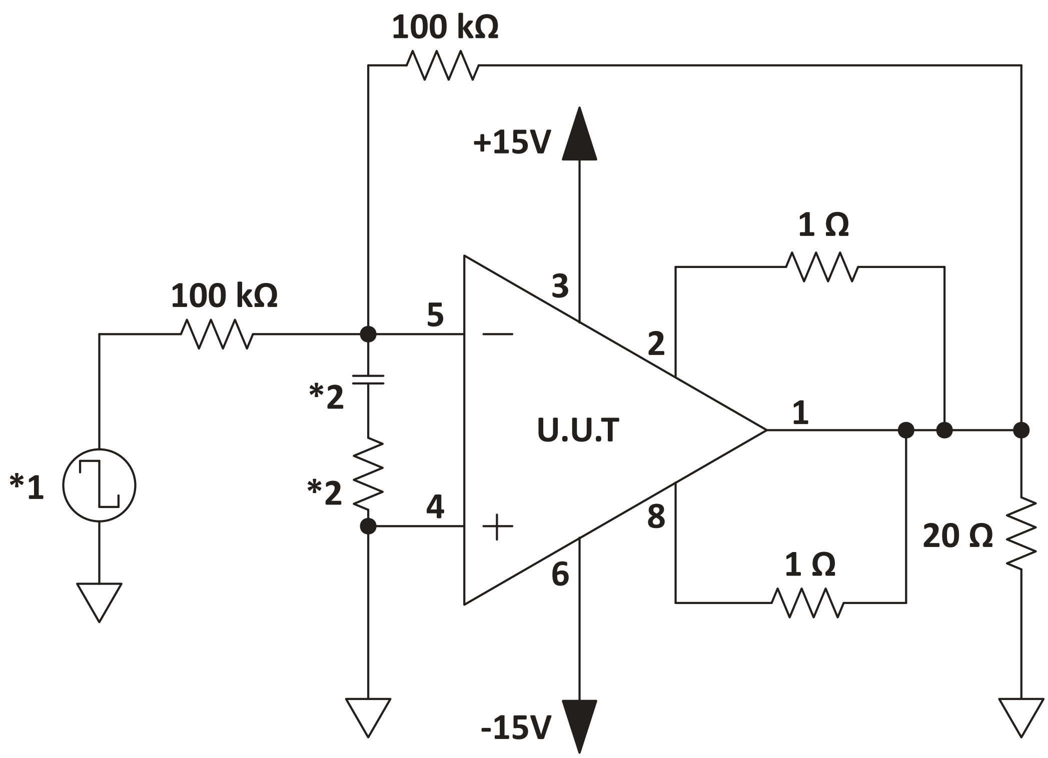
SG	Parameter	Symbol	Temp.	Power	Test Conditions	Min	Max	Units
1	Quiescent Current	I_Q	25°C	±40V	V_{IN}=0, A_V=100, R_{CL}= 0.1 Ω		50	mA
1	Input Offset Voltage	V_{OS}	25°C	±40V	V_{IN} = 0, A_V = 100		±6	mV
1	Input Offset Voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±12	mV
1	Input Offset Voltage	V_{OS}	25°C	±45V	V_{IN} = 0, A_V = 100		±7	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Input Bias Current,–IN	$-I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Input Offset Current	I_{OS}	25°C	±40V	V_{IN} = 0		±30	nA
3	Quiescent Current	I_Q	–55°C	±40V	V_{IN}=0, A_V=100, R_{CL}= 0.1 Ω		100	mA
3	Input Offset Voltage	V_{OS}	–55°C	±40V	V_{IN} = 0, A_V = 100		±11.2	mV
3	Input Offset Voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±17.2	mV
3	Input Offset Voltage	V_{OS}	–55°C	±45V	V_{IN} = 0, A_V = 100		±12.2	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±40V	V_{IN} = 0		±115	nA
3	Input Bias Current,–IN	$-I_B$	–55°C	±40V	V_{IN} = 0		±115	nA
3	Input Offset Current	I_{OS}	–55°C	±40V	V_{IN} = 0		±115	nA
2	Quiescent Current	I_Q	125°C	±40V	V_{IN}=0, A_V=100, R_{CL}= 0.1 Ω		50	mA
2	Input Offset Voltage	V_{OS}	125°C	±40V	V_{IN} = 0, A_V = 100		±12.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±18.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±45V	V_{IN} = 0, A_V = 100		±13.5	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input Bias Current,–IN	$-I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input Offset Current	I_{OS}	125°C	±40V	V_{IN} = 0		±70	nA
4	Output Voltage, I_O = 10A	V_O	25°C	±16V	R_L = 1 Ω	10		V
4	Output Voltage, I_O = 80mA	V_O	25°C	±45V	R_L = 500 Ω	40		V
4	Output Voltage, I_O = 5A	V_O	25°C	±35V	R_L = 6 Ω	30		V
4	Current Limits	I_{CL}	25°C	±14V	R_L = 6 Ω, R_{CL} = 1 Ω	0.6	0.89	A
4	Stability/Noise	E_N	25°C	±40V	R_L = 500 Ω, C_L = 1.5nF [1]		1	mV
4	Slew Rate	SR	25°C	±40V	R_L = 500 Ω	2.5	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±40V	R_L = 500 Ω, F = 10Hz	96		dB
4	Common Mode Rejection	CMR	25°C	±15V	R_L = 500 Ω, F = DC, V_{CM} = ±9V	74		dB

SG	Parameter	Symbol	Temp.	Power	Test Conditions	Min	Max	Units
6	Output Voltage, I_O = 8A	V_O	–55°C	±14V	R_L = 1 Ω	8		V
6	Output Voltage, I_O = 80mA	V_O	–55°C	±45V	R_L = 500 Ω	40		V
6	Stability/Noise	E_N	–55°C	±40V	R_L = 500 Ω, C_L = 1.5nF, [1]		1	mV
6	Slew Rate	SR	–55°C	±40V	R_L = 500 Ω	2.5	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±40V	R_L = 500 Ω, F = 10Hz	96		dB
6	Common Mode Rejection	CMR	–55°C	±15V	R_L = 500 Ω, F = DC, V_{CM} = ±9V	74		dB
5	Output Voltage, I_O = 8A	V_O	125°C	±14V	R_L = 1 Ω	8		V
5	Output Voltage, I_O = 80mA	V_O	125°C	±45V	R_L = 500 Ω	40		V
5	Stability/Noise	E_N	125°C	±40V	R_L = 500 Ω, C_L = 1.5nF, [1]		1	mV
5	Slew Rate	SR	125°C	±40V	R_L = 500 Ω	2.5	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±40V	R_L = 500 Ω, F = 10Hz	96		dB
5	Common Mode Rejection	CMR	125°C	±15V	R_L = 500 Ω, F = DC, V_{CM} = ±9V	74		dB

1. Minimum gain recommendation is either G = +4 (non-inverting) or G = –3 (inverting).

BURN IN CIRCUIT

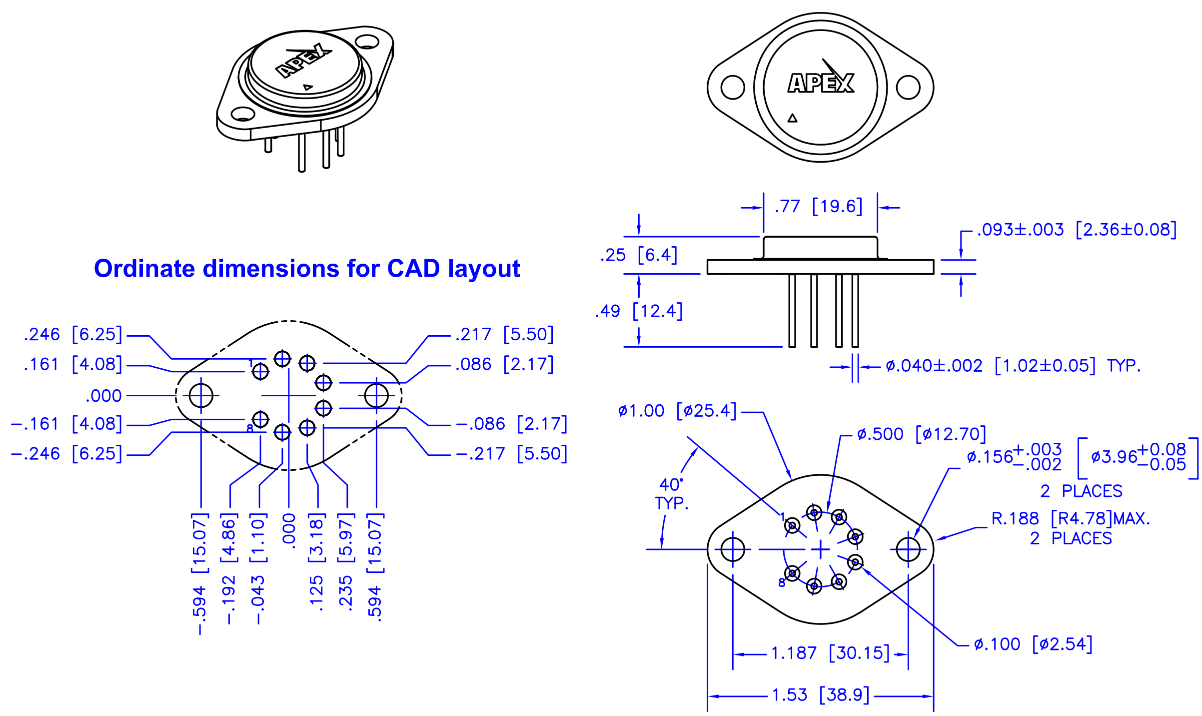
Figure 17: Burn In Circuit



1. Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.
2. These components are used to stabilize device due to poor high frequency characteristics of burn in board

PACKAGE OPTIONS

PACKAGE STYLE CE



NOTES:

1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Header flatness within pin circle is .0005" TIR, max.
4. Header flatness between mounting holes is .0015" TIR, max.
5. Standard pin material: Solderable nickel−plated Alloy 52.
6. Header material: Nickel−plated cold−rolled steel.
7. Welded hermetic package seal
8. Isolation: 500 VDC any pin to case.
9. Package weight: .53 oz [15 g]

NEED TECHNICAL HELP? CONTACT APEX SUPPORT!

For all Apex Microtechnology product questions and inquiries, call toll free 800-546-2739 in North America. For inquiries via email, please contact apex.support@apexanalog.com. International customers can also request support by contacting their local Apex Microtechnology Sales Representative. To find the one nearest to you, go to www.apexanalog.com