AIC1532

32-Channel High Voltage Driver

RoHS COMPLIANT

FEATURES

- 32 High Voltage Push-Pull Output Channels
- High Voltage up to 230V
- TTL compatible inputs
- Over-current and short-circuit protection
- Adjustable switching speed of the high voltage output
- Under-Voltage Protection

APPLICATIONS

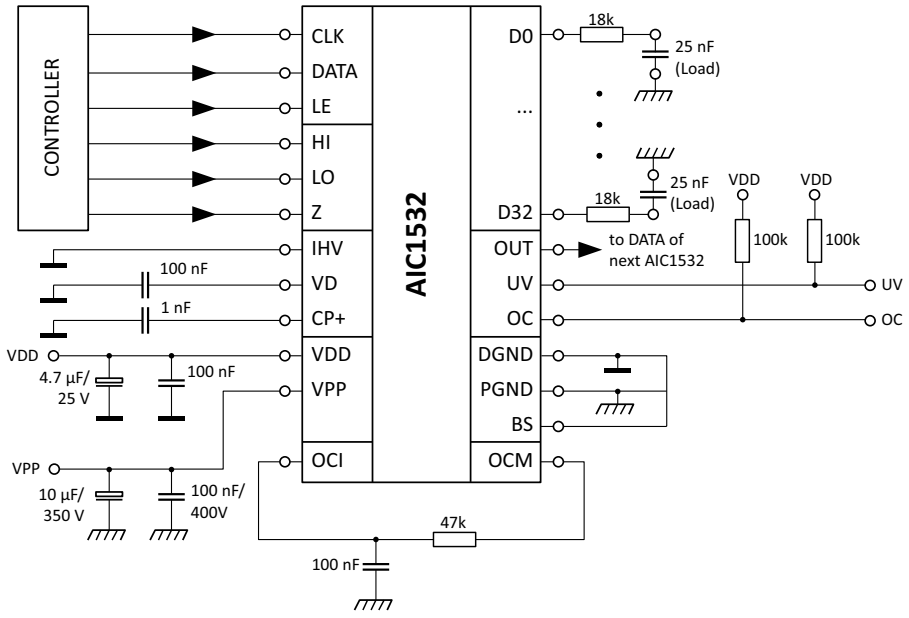
- Drive of Capacitive Actuators
- Piezo Transducer Excitation
- Electro-Luminescent Displays

DESCRIPTION

The AIC1532 is a 32 bit serial to parallel converter IC with 32 high voltage push-pull outputs and TTL compatible input signals.The outputs are designed can drive capacitive and resistive loads. An internal protection function monitors the logic supply voltage (VDD) and disables all output transistors of the high voltage push-pull outputs if an undervoltage condition is detected.

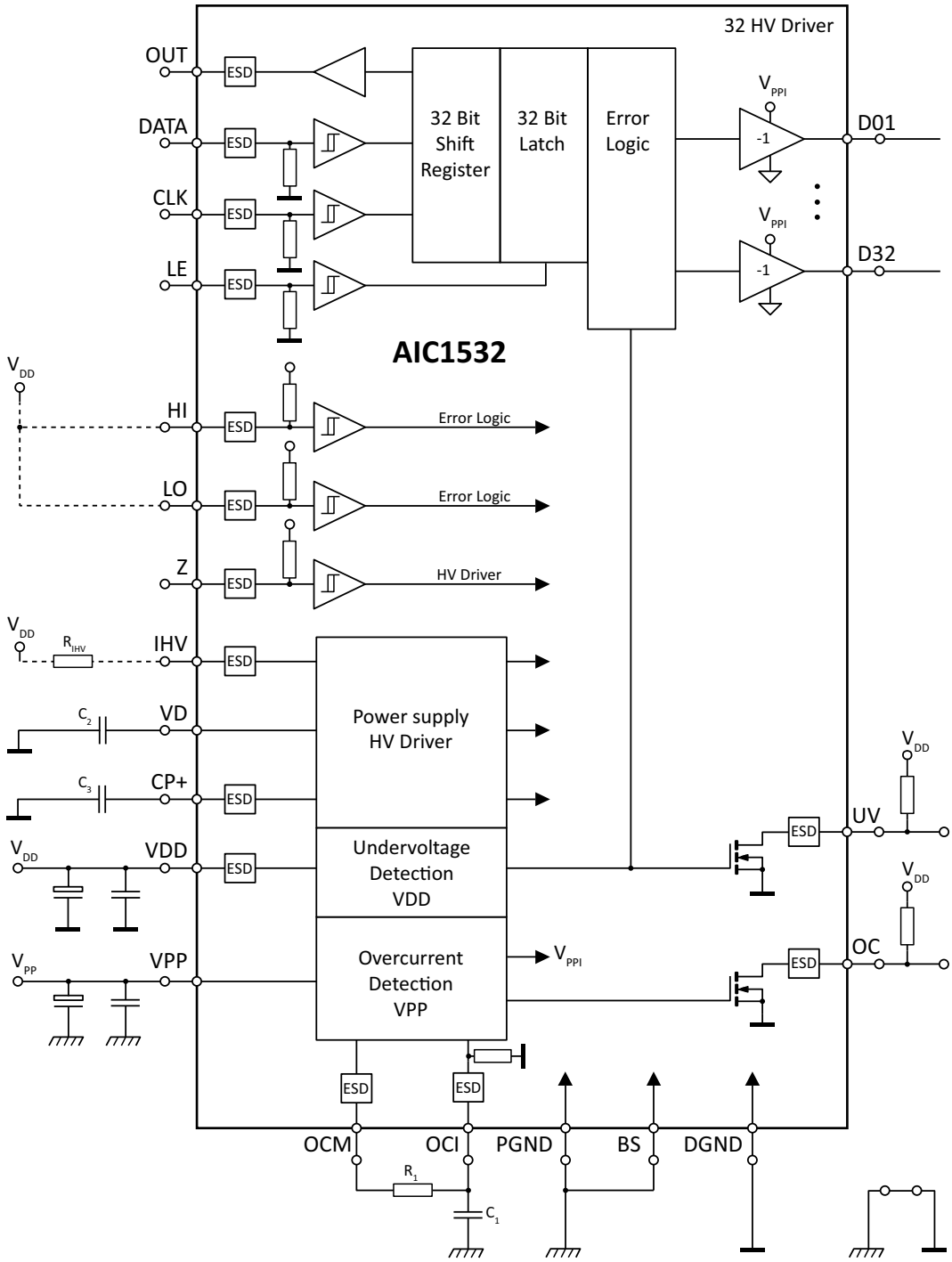
The IC contains a 32 bit shift register with a clock (CLK) and a data (DATA) input. The data output (OUT) allows cascading of several ICs. The 32 bit data will be latched with the Latch Enable Signal (LE) in a 32 bit latch. Three dedicated logic input signals (HI, LO, Z) allow setting of all high voltage outputs instantaneously to high, low, or high-impedance without changing the setting of the 32 bit shift register and latch.

Figure 1: Simple Application Circuit



BLOCK DIAGRAM

Figure 2: Block Diagram



PINOUT AND DESCRIPTION TABLE

Pin Number	Name	Description
1	D01	High voltage push-pull output 01
2	D02	High voltage push-pull output 02
3	D03	High voltage push-pull output 03
4	D04	High voltage push-pull output 04
5	D05	High voltage push-pull output 05
6	D06	High voltage push-pull output 06
7	D07	High voltage push-pull output 07
8	D08	High voltage push-pull output 08
9	D09	High voltage push-pull output 09
10	D10	High voltage push-pull output 10
11	D11	High voltage push-pull output 11
12	D12	High voltage push-pull output 12
13	D13	High voltage push-pull output 13
14	D14	High voltage push-pull output 14
15	D15	High voltage push-pull output 15
16	D16	High voltage push-pull output 16
17	NC	not connected
18	OCI	Input of the over current detection logic
19	NC	not connected
20	OCM	Output of the over current detection measurement circuit
21	NC	not connected
22	VPP	Power supply of the 32 high voltage push-pull outputs
23	NC	not connected
24	NC	not connected
25	DGND	Digital ground. Both DGND Pins must be connected together.
26	NC	not connected
27	PGND	Power ground of the 32 high voltage push-pull outputs. PGND must be externally connected to DGND, but avoid creating ground loops.
28	NC	not connected
29	NC	not connected
30	OC	Status output of the over current detection
31	NC	not connected
32	BS	Backside of the chip
33	D17	High voltage push-pull output 17
34	D18	High voltage push-pull output 18

35	D19	High voltage push-pull output 19
36	D20	High voltage push-pull output 20
37	D21	High voltage push-pull output 21
38	D22	High voltage push-pull output 22
39	D23	High voltage push-pull output 23
40	D24	High voltage push-pull output 24
41	D25	High voltage push-pull output 25
42	D26	High voltage push-pull output 26
43	D27	High voltage push-pull output 27
44	D28	High voltage push-pull output 28
45	D29	High voltage push-pull output 29
46	D30	High voltage push-pull output 30
47	D31	High voltage push-pull output 31
48	D32	High voltage push-pull output 32
49	Z	Input to switch off all the lower and the upper transistors of the high voltage push-pull outputs (high impedance status)
50	NC	not connected
51	HI	Input to switch all the high voltage push-pull outputs in the high state
52	LO	Input to switch all the high voltage push-pull outputs in the low state
53	LE	Input to set the 32 latches and reset the flip-flop of the over current signal
54	CLK	Input to clock the shift register
55	DATA	Data input of the shift register
56	IHV	Input to connect an external resistor to adjust the switching speed of the high voltage push-pull outputs. If not used, pin must be connect to DGND
57	DGND	Digital ground. Both DGND Pins must be connected together
58	UV	Status output of the under voltage detection
59	CP+	Connection for the external low-pass capacitor of the under voltage detection
60	OUT	Output to the cascading the IC for the next DATA Pin
61	VDD	Power supply for the digital logic
62	NC	not connected
63	VD	Gate voltage - block capacitor for the internal driver voltage of the output stages (without any external load)
64	NC	not connected

SPECIFICATIONS

Unless otherwise noted: T_{AMB} = 25°C, high voltage supply V_{PP} = 190 V, logic supply V_{DD}= 5 V, IHV connected to DGND.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
High voltage supply	V_{PP}	V_{DD}	280	V
Output voltage of the high voltage push-pull outputs	V_{DN}	-0.3	280	V
Logic supply voltage	V_{DD}	-0.3	7	V
Slew rate of V_{PP}			160	V/ms
Logic input levels	V_{IN}	-0.3	V_{DD}+0.3	V
Logic output levels	V_O	-0.3	V_{DD}+0.3	V
Output currents of the status outputs (under-voltage and over-current detection)	I_O		6	mA
Gate voltage	V_D	-0.3	13	V
ESD – protection [1]	V_{ESD}	-2000	+2000	V
Continuous total power dissipation	P_{TOT}		750	mW
Storage temperature range	T_{STG}	-55	150	°C
Junction temperature range	T_J	-25	150	°C
Thermal resistance	R_{THJA}		70	K/W

1. See Figure 2 for details on which pins are ESD protected

NORMAL OPERATING RANGE

Parameter	Symbol	Min	Typ	Max	Units
High voltage supply	V_{PP}	30	190	230	V
Logic supply voltage	V_{DD}	4.5	5.0	5.5	V
Slew rate of V_{PP} [1]				100	V/ms
High level input voltage	V_{INH}	2.0		V_{DD}	V
Low level input voltage	V_{INL}	0		0.8	V
Input voltage OCI On	V_{OCIE}	2.5		V_{DD}	V
Input voltage OCI Off	V_{OCIA}	0		2.0	V
Operating junction temperature	T_J	0		125	°C
Operating temperature	T_{AMB}	0		70	°C

1. During a data latch sequence V_{PP} must be stable.

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Quiescent supply current of the push-pull outputs	I_{PPQ}	V_{IN} = 0.1 V at HI, DATA, CLK, LE; V_{IN} = V_{DD}-0.5 V at LO, Z		0.15	0.60	mA
Supply current of the push-pull outputs by D01 – D32 = Low	$I_{PP,ON}$	V_{IN} = 0.1 V at LO, DATA, CLK, LE; V_{IN} = V_{DD}-0.5 V at HI, Z		0.50	1.00	mA
Quiescent supply current of the logic	I_{DDQ}	V_{IN} = 0.1 V at DATA, CLK, LE; V_{IN} = V_{DD}-0.5 V at HI, LO, Z		0.15	0.30	mA
Supply current of the logic	I_{DD}	f_{CLK} = 2 MHz; f_{Data} = 1 MHz		0.50	5.00	mA
High level input current at HI, LO, Z	$-I_{IN,H}$	$V_{IN,H}$ = V_{DD}-0.5 V			30	µA
Low level input current at HI, LO, Z	$-I_{IN,L}$	$V_{IN,L}$ = 0.1 V			200	µA
High level input current at DATA, CLOCK, LE	$I_{IN,H}$	$V_{IN,H}$ = V_{DD}-0.5 V			100	µA
Low level input current at DATA, CLOCK, LE	$I_{IN,L}$	$V_{IN,L}$ = 0.1V			10	µA
High level input current at OCI	$I_{OCI,H}$	$V_{OCI,H}$ = V_{DD}-0.5 V			30	µA
Low level input current at OCI	$I_{OCI,L}$	$V_{OCI,L}$ = 0.1 V			10	µA
Low level output for OUT, OCM	$V_{OUT,L}$	I_{OUT} = 100 µA			0.5	V
High level output for OUT, OCM	$V_{OUT,H}$	$-I_{OUT}$ = 100 µA	V_{DD}-1			V
Low level output for OC, UV	$V_{O,L}$	I_D = 5mA, VDD = 2.9 V			1	V
Switching level of the over current detection at VPP	I_{VPPU}	Measured to toggle at High on OCM; V_{OCI} = 0.1 V	2		5	mA

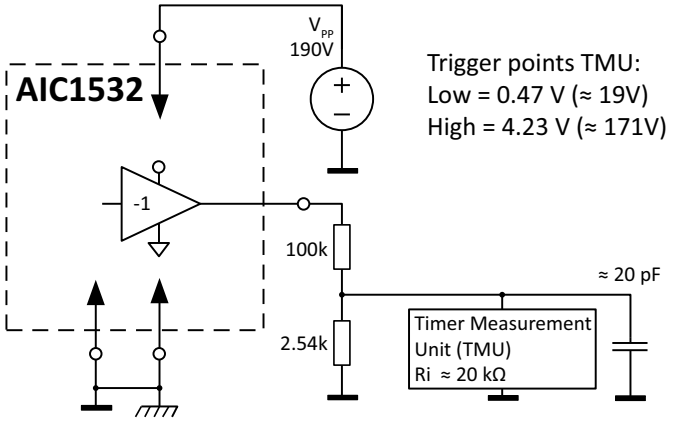
Under voltage level (down)	V_{UV-}		3	3.4	3.8	V
Under voltage level (up)	V_{UV+}		3.4	3.9	4.4	V
Residual current of one upper output transistor	$-I_{R,OT}$	V_{DS} = 190 V; V_{IN} = V_{DD}; V_Z = 0 V			10	µA
Residual current of one lower output transistor	$I_{R,UT}$				10	µA
Voltage drop over one upper output transistor	$\Delta V_{D,OT}$	I_D = 6.5 mA; V_{OCI} = 0.1 V		6.5	10	V
Voltage drop over one lower output transistor	$\Delta V_{D,UT}$			2.5	10	V
Minimal output current of one upper output transistor	$-I_{Dmin,OT}$	V_{DS} = 30 V; V_{OCI} = 0.1 V	20			mA
Minimal output current of one lower output transistor	$I_{Dmin,UT}$		20			mA

AC CHARACTERISTICS

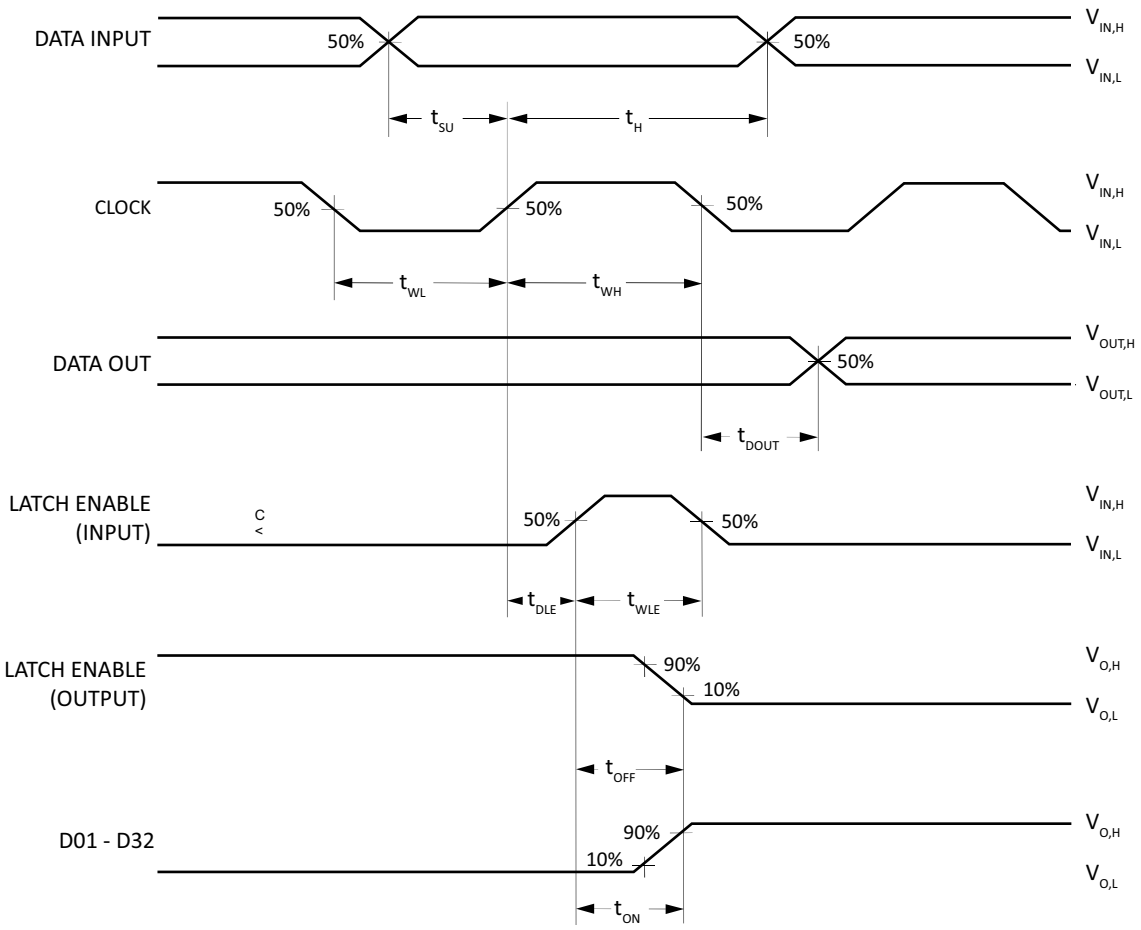
See also section *SWITCHING WAVEFORMS* for illustration

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Clock frequency	f_{CLK}				2	MHz
Clock width high	t_{WH}		100			ns
Clock width low	t_{WL}		100			ns
Data setup time before clock rises [1]	t_{SU}		30			ns
Delay time clock to OUT	t_{DOUT}				40	ns
Data hold time before clock rises	t_H	C_L = 20pF (Lab) or [2]	50		$t_{WH}/2$	ns
LE delay time after rising edge of clock	t_{DLE}		10			ns
Width of latch enable pulse	t_{WLE}		50			ns
Rise- and fall time of D01 - D32	t_{ON}, t_{OFF}				75	µs

1. Data setup only during in the low phase of clock
2. Principle measurement of rise and fall time of D01 - D32 with test measurement unit (TMU):



SWITCHING WAVEFORMS



OPERATING FUNCTION TABLE

Function	Inputs [1]							Outputs [2]			
	CLK	DATA	LE	LO	HI	Z	OCI	OUT	D	OC	UV
LO Mode	X	X	X	L	H	H	L	*	L	H	H
HI Mode	X	X	X	H	L	H	L	*	H	H	H
Z Mode	X	X	X	X	X	L	L	*	Z	H	H
Load SR	↑	X	L	H	H	H	L	*	*	H	H
Store	X	X	↑	H	H	H	L	*	*	H	H
Transparent Latch	↑	L	H	H	H	H	L	*	L	H	H
Mode	↑	H	H	H	H	H	L	*	H	H	H
Over Current OCI	X	X	X	X	X	X	H	*	L	L	H

1. L = low, H = high, X = irrelevant, ↑ = low to high transition
2. L = low, H = high, Z = high impedance, * = dependent from previous CLK or LE status. OCI has the highest priority.

TYPICAL PERFORMANCE GRAPHS

Figure 3: Dependency of T_{ON}, T_{OFF} from ambient Temperature

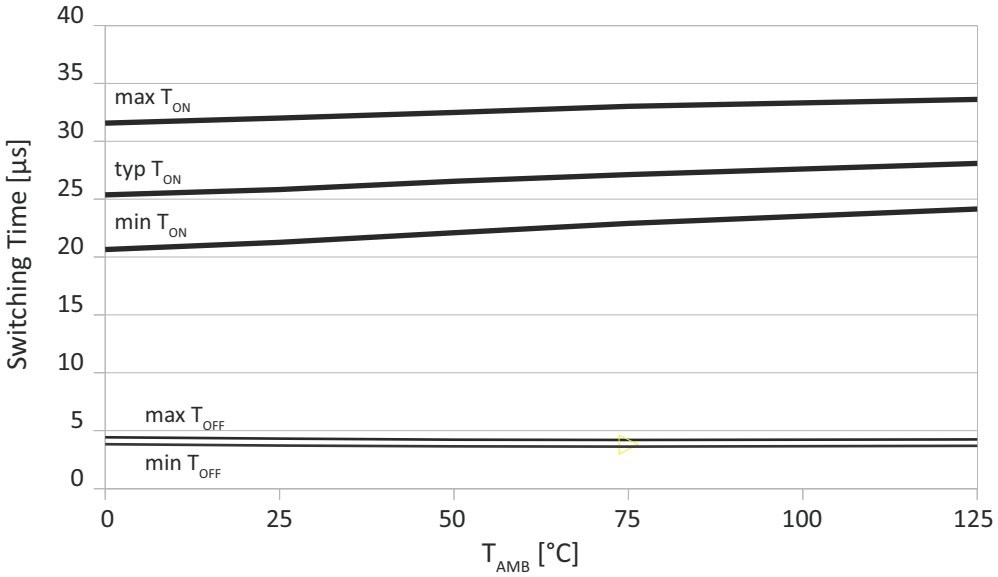
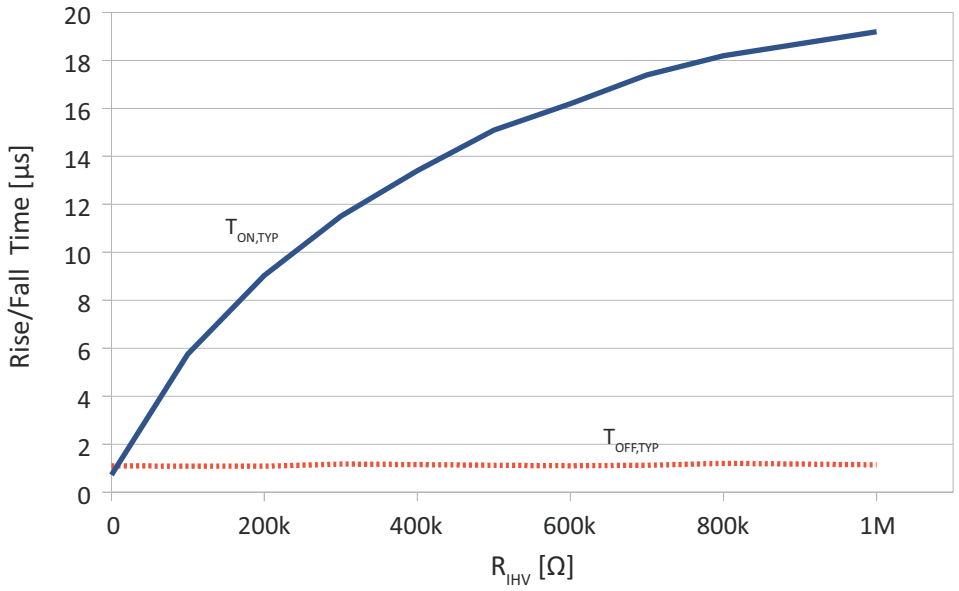
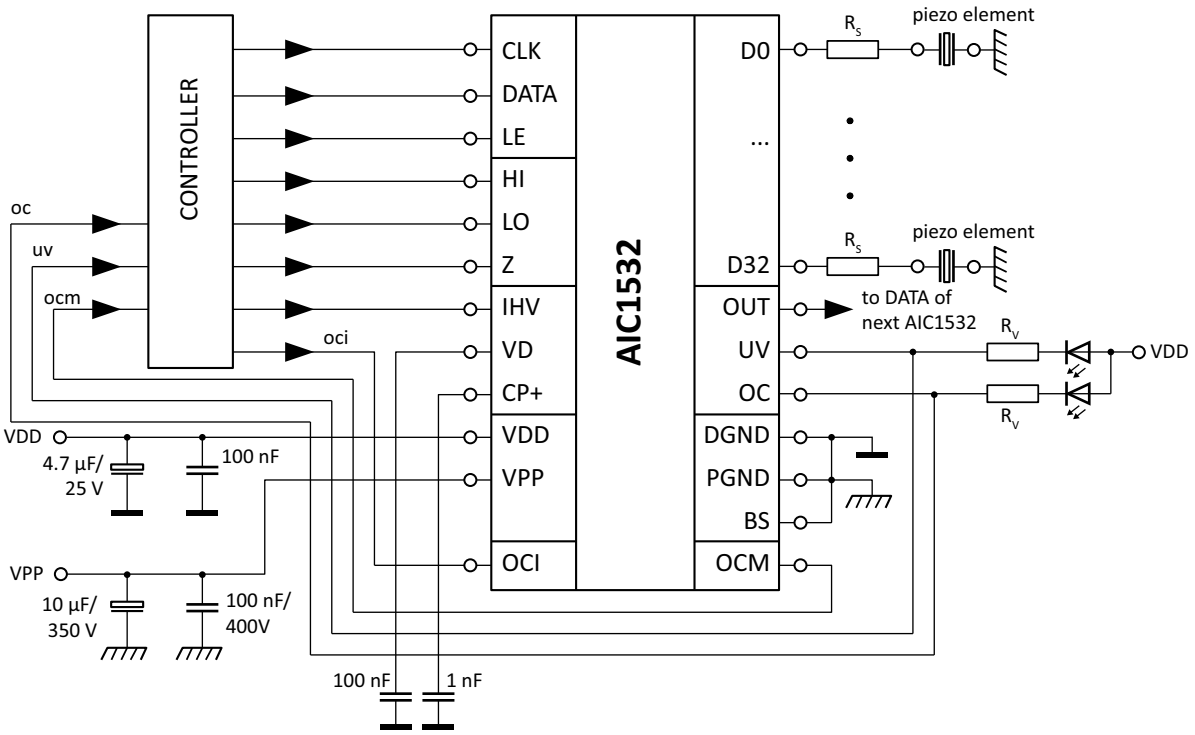


Figure 4: Dependency of T_{ON}, T_{OFF} from IHV Resistance



APPLICATION

Figure 5: Example Application Circuit



OVER-CURRENT DETECTION

AIC1532 includes an over-current detection circuit of the voltage supply of the high voltage push-pull outputs. The signal of the over-current detection can delayed or noise filtered by an external R-C combination. AIC1532 provides an over-current measuring output (OCM) and an over-current input (OCI) signal. By activation of the over-current input (OCI) a flip-flop will be set, switching the high voltage push-pull outputs to the low state. The over-current flip-flop can be reset by applying the latch enable signal (LE). To display the over current a status output (OC) exist according to the logic table. It is possible to connect this output parallel with other (OC) outputs (wired or).

UNDER-VOLTAGE DETECTION

If the logic voltage supply falls below a threshold of about 4 V, the under-voltage detection will be activated and the transistors of the high voltage push-pull outputs turns off. To display an under-voltage condition, an output (UV) is activated (pulled to low), indicating that the logic voltage supply is to small for a secure function of the internal logic. It is possible to connect this output parallel with other (UV) outputs (wired or). The capacitor on (CP+) serve as a noise filter capacitance for the under-voltage detection.

OTHER FUNCTIONS

The high voltage push-pull outputs are protected against a possible latch-up by using the drain diodes of the output high voltage transistors and their complete dielectric isolation.

The switching speed of the high voltage push-pull outputs is adjustable by adding an external resistance R_{IHV} between pin (IHV) and the logic voltage supply (VDD). If no speed adjustment is desired, the pin (IHV) must be connected to the digital ground (DGND).

AIC1532 includes an interval power supply for the high voltage push-pull driver, requiring an external stabilization capacitor connected to pin (VD). To ensure reliable operation, pin (VD) must not be connected to any external loads.

All inputs and the low voltage outputs are protected against electrostatic discharge (ESD) up to ± 2000 V.

LIMITATIONS FOR THE LOAD SERIES RESISTOR AND THE LOAD CAPACITANCE

To protect AIC1513 against thermal over-stress, the series resistor to the connected load (R_S) and the capacitance of the connected load (C_S) need to meet the following two criteria:

$$R_S \geq \frac{V_{PP}}{10mA}$$

and

$$C_S \leq \frac{5ms}{R_S}$$

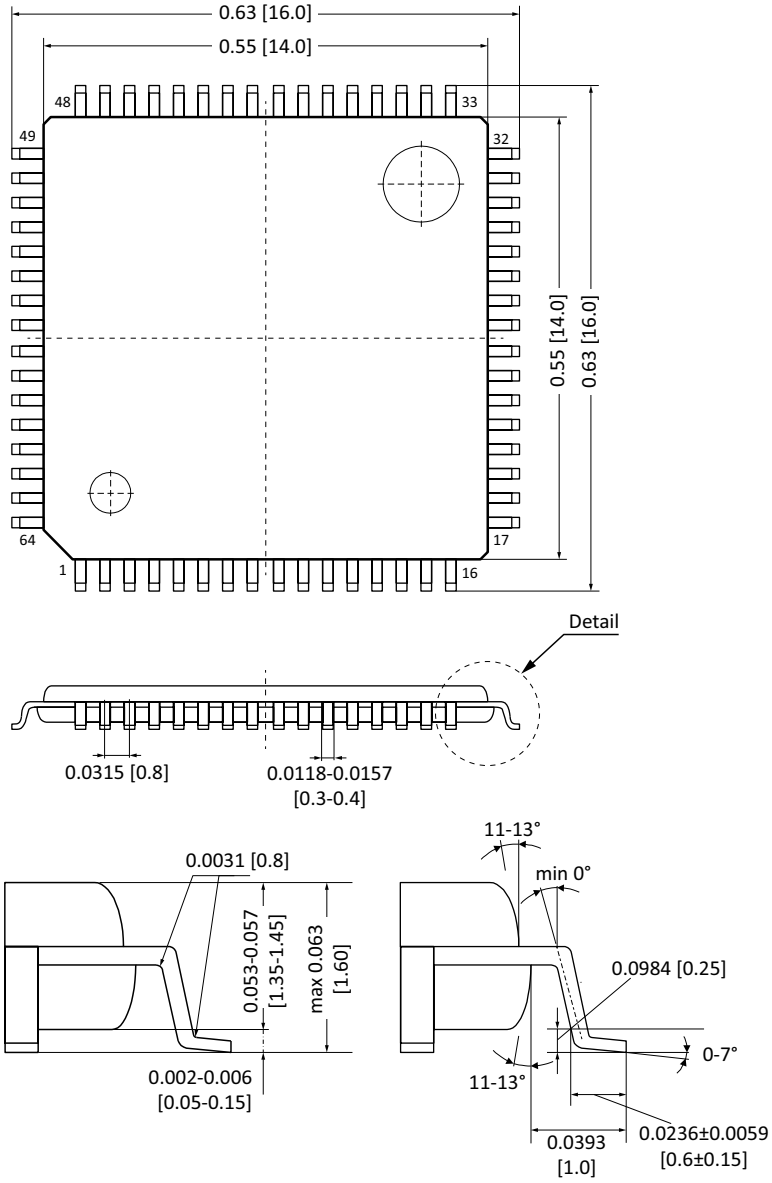
NOISE OR DELAY FILTER FOR OVER-CURRENT PROTECTION

The time constant for a noise or delay filter for the over-current protection must be set to less than 5 ms (see Figure 2 for illustration of placement for R_1 and C_1):

$$\tau = R_1 \times C_1 \leq 5ms$$

PACKAGE OPTIONS

Part Number	Apex Package Style	Description
AIC1532	ZD	64-pin LQFP



ESD PROTECTION

The Requirements for Handling Electrostatic Discharge Sensitive Devices are described in the JEDEC standard JESD625-A. Please note the following recommendations:

- When handling the device, operators must be grounded by wearing a for the purpose designed grounded wrist strap with at least 1M? resistance and direct skin contact.
- Operators must at all times wear ESD protective shoes or the area should be surrounded by for ESD protection intended floor mats.
- Opening of the protective ESD package that the device is delivered in must only occur at a properly equipped ESD workbench. The tape with which the package is held together must be cut with a sharp cutting tool, never pulled or ripped off.
- Any unnecessary contact with the device or any unprotected conductive points should be avoided.
- Work only with qualified and grounded tools, measuring equipment, casing and workbenches.
- Outside properly protected ESD-areas the device or any electronic assembly that it may be part of should always be transported in EGB/ESD shielded packaging.

STORAGE CONDITIONS

The AIC1532 meets moisture sensitivity classification MSL2, according to JEDEC standard J-STD-020, and should be handled and stored according to J-STD-033.