Use High-Voltage Op Amps To Drive Power MOSFETs

Meet the distortion and stability requirements using the proper combination of op amps and power MOSFETs

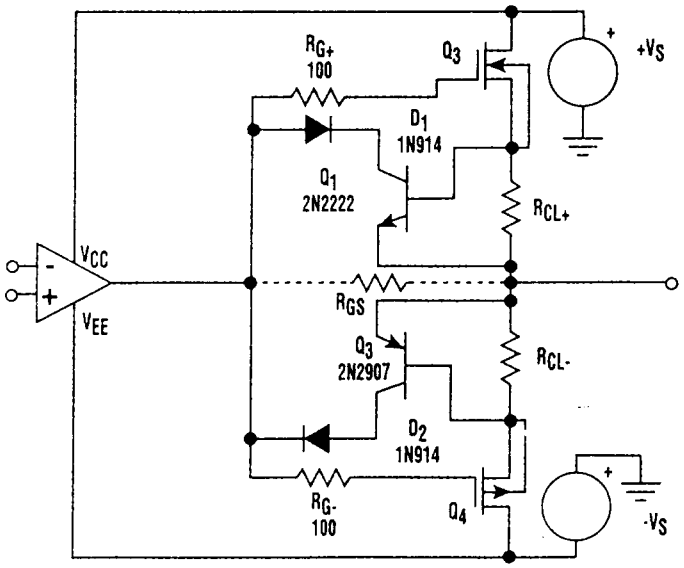
BY JERRY STEELE and DENNIS EDDLEMON
Apex Microtechnology Corp.

Although high-voltage op amps can operate from supplies ranging from 100 up to 450 V, their output currents generally are limited to less than 200 mA. When the need arises to deliver several amperes of current at high voltages, the designer must add some type of buffering for the op amps, such as external MOSFETs. Therefore, protecting the MOSFETs while still meeting distortion and stability requirements must be a priority during design.

The choice of which MOSFETs to employ is determined entirely by current, voltage, and power-dissipation requirements. There are no radical differences among the different MOSFETs regarding threshold voltages or transconductance.

In applications where distortion isn't important, a simple circuit will suffice, such as one that ties each MOSFET base together and connects the bases to the op amp's high-voltage output *(Fig. 1)*. This connection will suffer from crossover distortion, but for dc or applications below 1 kHz, it's generally not a problem. Note that 100-Ω gate resistors should always be placed physically close to the gate pin.

To reduce crossover distortion, simply add a gate-source resistance, R_{GS}. This is possible because most high-voltage op amps employed in these applications can handle significant currents, usually over 60 mA. The resistor, in effect, lets the driving op amp supply low values of load current until the drop across the resistor reaches the MOSFETs' threshold voltage. Then, there's a smooth transition to the MOSFETs supplying the dominant current.

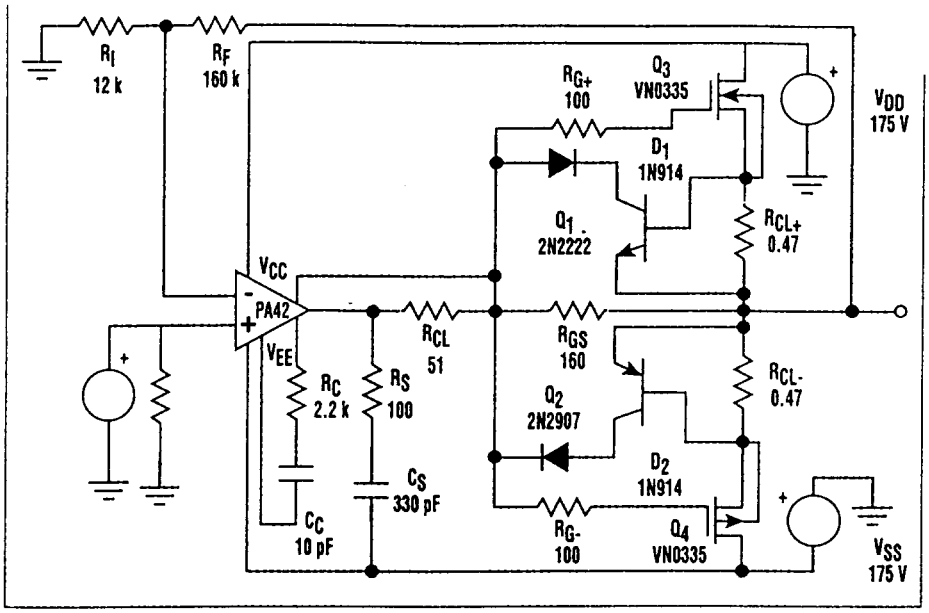


1 To build a circuit in which distortion isn't an issue, tie each MOSFET base together and connect that point to the output of the high-voltage op amp. To reduce crossover distortion, add a gate-source resistance, R_{GS}, to the circuit (as shown with dotted lines in the circuit).

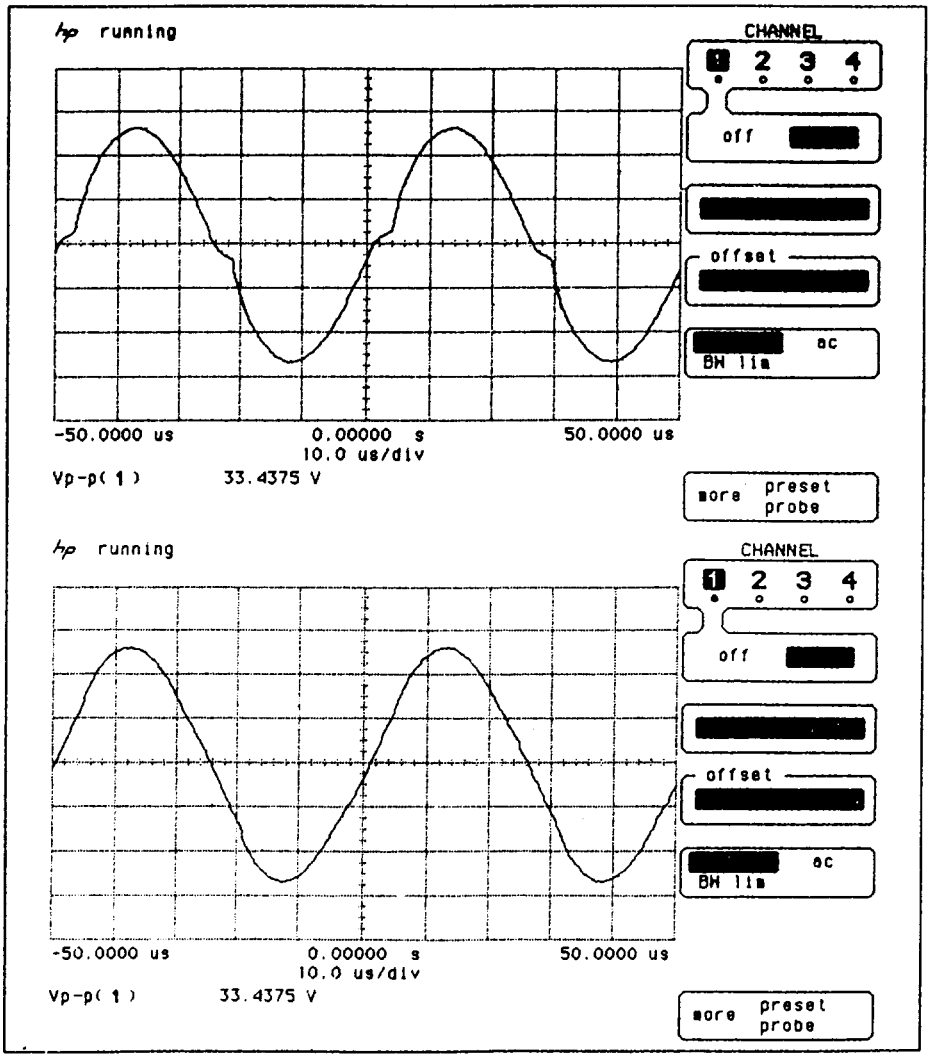
The R_{GS} resistor should be as low in value as is practical. Choosing the right R_{GS} guarantees that the maximum required gate-drive voltage coincides with the driver op amp's current limit. This helps ensure that the MOSFET gate will never be overdriven. For example, the Apex Microtechnology PA42 power op amp is rated for a maximum output current of 60 mA, and it would be current limited at that value. A 10-V maximum gate drive requirement will result in a 160-Ω resistor.

Transition of current to the output MOSFETs occurs at the MOSFET threshold voltage of about 3 V. With the 160-Ω resistor, this occurs at a load current of 18 mA. As the resistor value increases, the distortion reduction benefits become less significant. Setting the driver op amp for the highest possible current results in the lowest distortion because R_{GS} can be minimized.

To evaluate this technique's performance, the PA42 was selected to drive a pair of 3-A power MOS-



2 This 175-V high-current amplifier circuit was used to evaluate the performance of a distortion-reduction technique. The PA42 drives the two power MOSFETs.



3 The high-current amplifier circuit's output becomes much cleaner by adding a 160-Ω gate-source resistor. The first plot (a) is taken without the resistor; the second (b) is with the resistor inserted.

FETs from Supertex, Sunnyvale, Calif. *(Fig. 2)*. The improvement gained by adding the 160-Ω R_{GS} can be observed in a plot of the output voltages, with and without the resistor connected in the circuit *(Figs. 3a and 3b)*.

To further quantify the effect of R_{GS}, actual distortion measurements were taken. At 1 kHz, with a 10-V rms output into 330 Ω, distortion was 0.62% without R_{GS} and 0.2% with it. The PA42 alone only accounts for 0.03% distortion at 1 kHz, so the added MOSFETs still increase distortion. But 0.2% is low enough for many applications.

A 40-V pk-pk square wave was driven into a 330-Ω resistive load to determine the effect on stability. A single cycle of overshoot with less than 30% of the total peak-to-peak amplitude was observed, which is indicative of a 30° phase margin, which is adequate.[1,2]

QUASI-COMPLEMENTARY OUTPUTS

Above 300 V, p-channel power MOSFETs can be difficult to find. An alternative is to use a quasi-complementary connection on the negative half of the n-channel MOSFET. In the circuit's topology, the selection of R_G will determine the maximum current flow through Q_1 *(Fig. 4)*. R_G is selected so that the voltage across R_G, under these conditions, corresponds to the maximum gate driver required at Q_3, which typically is around 10 V.

As a rule, the maximum current through Q_1 should not exceed 10% of the current in Q_3. For the best bandwidth performance, R_G should be kept low, with a value typically around 100 Ω.

When implementing the quasi-complementary connection with Class A/B biasing, R_G is selected so that Q_3 is never on under quiescent conditions. The voltage drop across R_G under quiescent conditions should be sufficiently below the threshold of Q_3. Then Q_3 would be in the off condition, even at temperature extremes.

CLASS A/B BIASING

Supplying an actual threshold voltage for the power MOSFETs, as would be done for traditional Class

A/B biasing, requires careful design to prevent thermal runaway. A common mistake is to rely on diodes or a bipolar transistor's V_{BE} multiplier to provide biasing for output devices that conduct some current along with temperature compensation. Simple diodes or bipolar transistors cannot properly compensate MOSFET gate-voltage temperature coefficients (TCs).

Thermal runaway occurs when the bias source's TC and the power MOSFETs' V_{GS} threshold don't match. Power MOSFETs have a positive TC of drain current versus V_{GS} at their threshold, which means drain current will increase with temperature.

This increased temperature further increases the current. Most power MOSFETs eventually have a negative TC of drain current versus gate voltage, but it occurs at very high currents. This condition most often results in destruction in linear circuit applications.

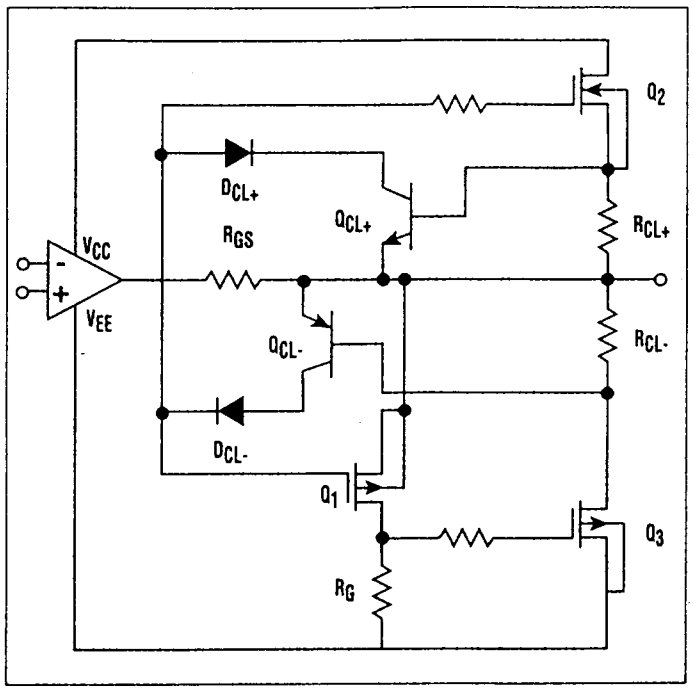
The biasing needed to reduce crossover distortion can be simplified by not turning on the output devices. With no bias and the typical MOSFET threshold of 3 V, it takes a 6-V swing to transition through the crossover region.

Any amount of bias will reduce crossover distortion. A simple diode-connected MOSFET (gate connected to drain) between the output device gates will often "absorb" much of this threshold.

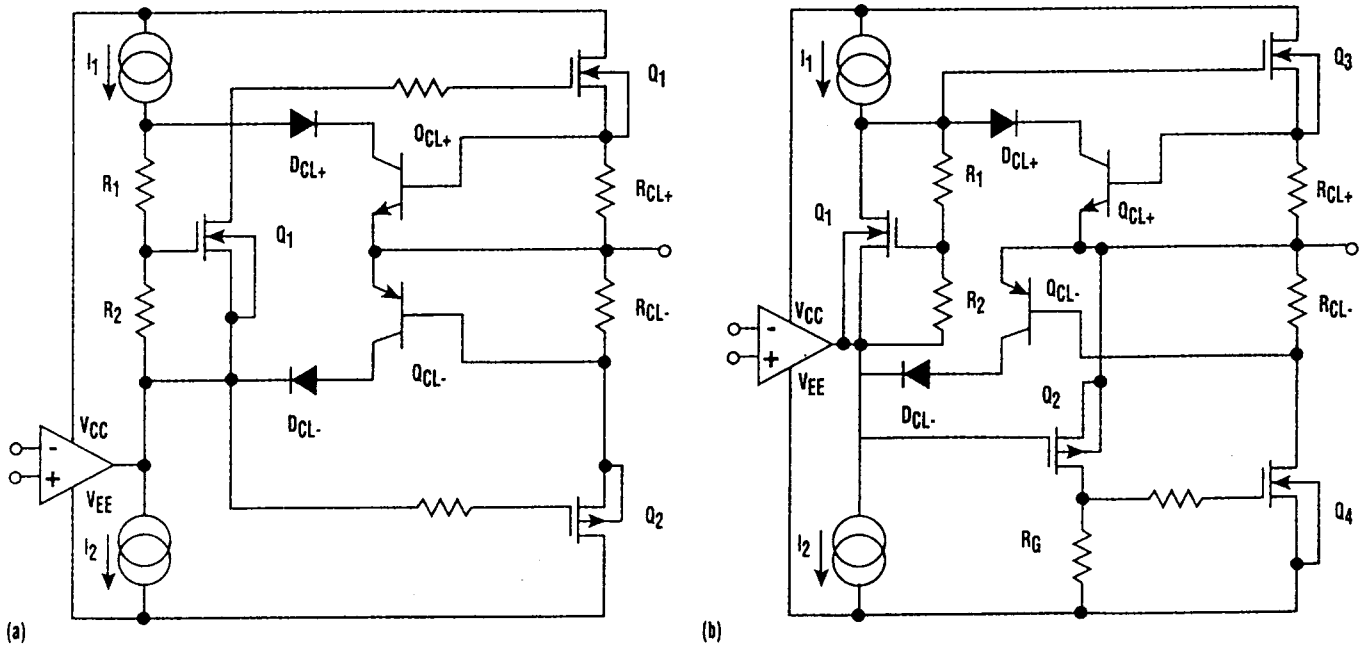
Using a V_{GS} multiplier is the only way to supply temperature-compensated biasing when the output devices must be turned on. The same MOSFET, MOSFET type, or geometry for the V_{GS} multiplier that's used for output devices should be employed. The V_{GS} multiplier circuit can be built with complementary-type outputs *(Fig. 5a)* or quasi-complementary-type outputs *(Fig. 5b)*. The distribution of current through the MOSFET and the parallel resistor divider is important because it will affect the TC. The TC will increase as more current is allowed to flow in the divider.

The V_{GS} multiplier requires a source of biasing current that could simply come from a pair of resistors or current sources. A stable TC of this current will simplify the design process, because the current's TC also affects the V_{GS} multiplier's ultimate TC.

In addition, if a single current source is used without a current return, that current must flow in the



4 By using a quasi-complementary circuit, the value of R_G can be kept as low as possible—around 100 Ω is reasonable.



5 A basic V_{GS} multiplier circuit can be built with either complementary-type outputs (a) or quasi-complementary-type outputs (b). The distribution of current through the MOSFET and the parallel resistor divider affects the temperature coefficient.

driver op amp's output circuit. The output can be connected to either side of the V_{GS} multiplier. However, if a single current source supplies the multiplier without a return path, the op amp must be connected opposite from the current source to provide a return path.

The design of a V_{GS} multiplier can only be arrived at empirically by experimenting on an actual working amplifier. It's essential that the chosen power output devices be curve-traced over temperature. That's because MOSFET data sheets don't supply information in enough detail to allow a prediction of low-current gate threshold behavior over temperature.

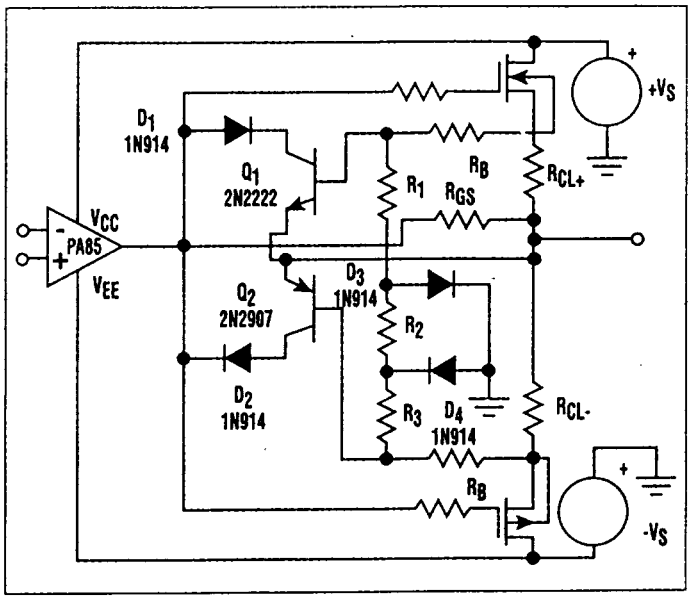
The ratio of the R_1-R_2 divider in the example circuit is adjusted to provide the desired quiescent current *(Fig. 5, again)*. In any real-world implementation, trimming must be used to set the output quiescent current. The output current will increase as the ratio of R_1/R_2 increases, which is done by raising R_1 or lowering R_2. The distribution of current between the divider and the MOSFET should then be optimized to achieve a zero or negative TC of current in the output MOSFETs. This becomes less critical over narrower temperature ranges.

Setting the output stage current as low as possible helps reduce output-stage transconductance and sensitivity to biasing, and is therefore easier to compensate. An actual example of Class A/B biasing is described later in the performance evaluation of several high-speed MOSFET drive circuit examples.

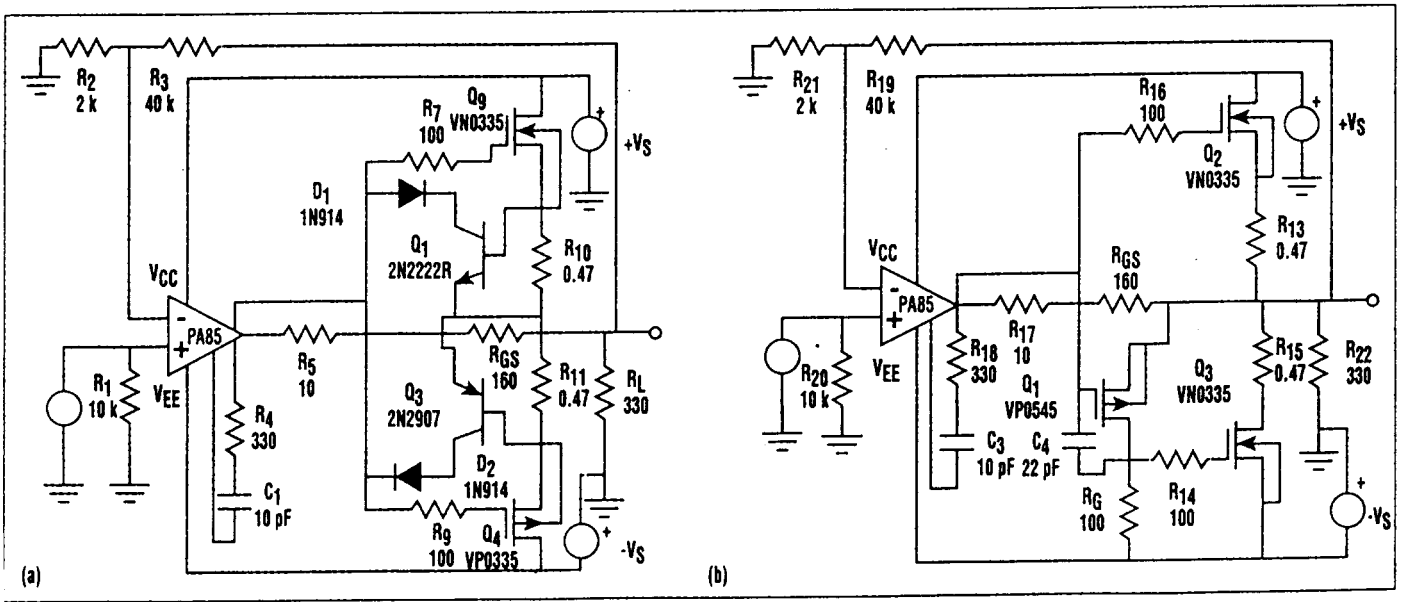
With a well-defined load (and generally a resistive one), additional protection circuitry may not be needed. However, many applications could be subjected to load variations or shorts, which require some type of current limiting on the buffer transistors. Simple current limiting is the easiest available option, in which a small-signal bipolar transistor senses the voltage drop across the MOSFET source resistor *(Fig. 1, again)*.

Activation occurs at 0.7 V ±20%. Some additional variation may occur, depending on which current-limit transistor is chosen. The diode in the collector circuit is needed to avoid forward-biasing the collector-base junction of the current-limit transistor on the side that is not delivering current. Otherwise, premature clipping of the output voltage swing would occur. Though Figure 1 shows two current-sense resistors, they could be combined into a single resistance.

Load line limiting, which provides a better match of current limit than what safe-operating area (SOA) limitations permit, can be implemented using a voltage divider circuit *(Fig.*



6 Load-line limiting can be handled using R_B as a voltage divider. For positive output swings, R_1 acts as the ground leg of the divider. For swings opposite the rail supplying current, the divider's ground leg consists of the series combination of R_2 and either R_1 or R_3.



7 Two high-speed circuits, one full complementary (a) and one quasi complementary (b), are based on the PA85 wideband high-voltage op amp. The two circuits show identical distortion numbers, but the output voltage swing of the quasi-complementary circuit was limited to 240 V pk-pk under identical conditions. The slew rate was also slower: 430 versus 360 V/μs.

6). For positive output swings, R_1 acts as the divider's ground leg, attenuating the current-limiting signal from the current-sense resistor as the output moves closer to the positive rail (as voltage stress across the power device decreases, more current is allowed). For swings that are opposite the rail supplying current, the divider's ground leg comprises the series combination of resistors R_2 and either R_1 or R_3.

The load-line-limit circuit allows a higher current limit when the output current's polarity corresponds to that of the voltage supply rail. The opposite-side current limit decreases and the divider action of resistors R_B and R_1 or R_3 plus R_2 must not permit the limiter on the rail opposite the rail supplying current to develop more than 0.7-V base drive.

Two high-speed circuits, one full complementary and one quasi complementary, were constructed based on the PA85 wideband high-voltage op amp *(Figs. 7a and 7b)*. The full-complementary circuit, with a gain of 20, provided the following performance (THD at ±275-V pk-pk output, 330-Ω load):

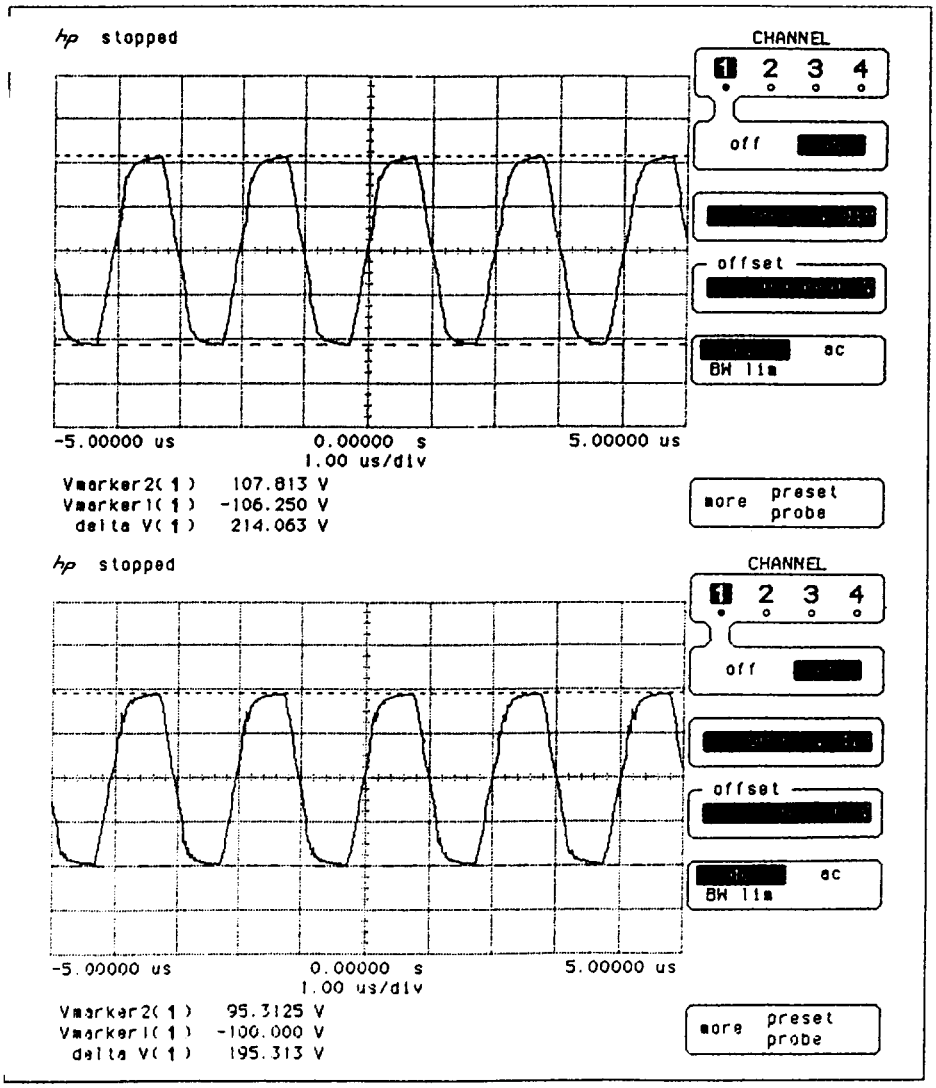
- At 50 kHz, THD is 0.35%;
- at 20 kHz, 0.17%;
- at 10 kHz, 0.1%;
- and at 1 kHz, 0.035%.
- Slew rate is 430 V/μs.

Square-wave performance shows adequate phase margin in either the complementary or quasi-complementary circuit *(Fig. 8)*. The quasi-complementary circuit exhibited identical distortion numbers, but the output voltage swing was limited to 240 V pk-pk under identical conditions. The slew rate on the quasi complementary circuit was also slower, at 360 V/μs.

The same circuit was reconfigured for Class A/B biasing. Through an iterative process, a V_{GS} multiplier using a Supertex VN0545 and a 1.5-kΩ R_2 was designed. The multiplier requires a 5-mA current that comes from two 30-kΩ resistors, each connected to a supply rail in the test circuit (rather than actual current sources). Resistor R_1 is a 1.5-kΩ potentiometer, which is adjusted to provide a current of 2.0 mA in the output devices.

With the PA85 as a driver amplifier, distortion was under 0.05% at all frequencies below 50 kHz. This design successfully compensates the output stage over a –25° to +85°C temperature range.

Finally, a note on boost for improved voltage swing: The output voltage swing from a circuit that uses MOSFETs as followers is inherently limited by the gate-voltage requirement. A simple way to improve the output swing is to better saturate the MOSFETs. This is done by running the driver op amp from power supplies with voltage levels 5 to 10 V greater than the output devices' drain voltages.



8 The square-wave performance of two circuits, the full complementary (top) and the quasi-complementary (bottom), shows, by the lack of overshoot, adequate phase margin.

References:
1. Landee, Davis, and Albrecht, *Electronic Designers' Handbook*, McGraw-Hill Books, 1957.

2. Huelsman, *Basic Circuit Theory With Digital Computations*, Prentice-Hall Inc., 1972.

DENNIS EDDLEMON, who has been dubbed the "Shah of High-Voltage Op Amps" by Bob Pease, is a design engineer for Apex Microtechnology Corp., 5980 N. Shannon Rd., Tucson, AZ 85741. Eddlemon holds a BA in sociology from Valparaiso University, Indiana.

JERRY STEELE is a senior applications engineer with Apex Microtechnology. He has over 15 years experience in electronics engineering, teaching, consulting, and delivering seminar presentations.