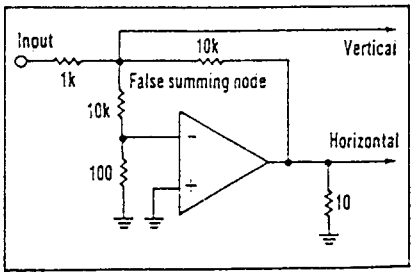
SIMPLE CIRCUIT DESIGN TECHNIQUES APPLIED TO NEW MOSFET POWER OP AMPS PRODUCE HIGH LINEARITY AND BANDWIDTH WITHOUT SACRIFICING ACCURACY AND STABILITY.

DESIGN TECHNIQUES FOR MOSFET POWER OP AMPS

Designers of shake table systems, function-generator output stages, and acoustic instruments require power amplifiers with wide bandwidths and low distortion. Although industrial-type power op amps can operate over a wide gain range and implement various transfer functions, their use in these applications requires compromising trade-offs of linearity and bandwidth against accuracy and stability. Fortunately, recent advances in power op-amp technology combined with a few simple circuit design principles can help maximize bandwidth and minimize distortion while maintaining accuracy and stability. Circuit design begins with choosing the proper amplifier, which can make a sizeable difference in performance.

Improvements in power op-amp technology have been sparked by an increase of demanding applications. For example, recent growth in sonar applications has created the need for a high power, highly linear amplifier with a power bandwidth of nearly 100 kHz. To supply this bandwidth with power levels in excess of 200 W, Apex uses power MOSFETs in its PA04 amplifier. The PA04, in contrast to previous MOSFET amplifier designs, has MOSFETs in all of its active gain stages as well as in the output stage, resulting in high linearity and bandwidth. This article focuses on the PA04, but the application techniques described are useful for any power op amp required to perform with optimum distortion and bandwidth characteristics.

The optimum combination of low distortion and wide bandwidth in power op amps is typified in the Apex PA04, a MOSFET-output amplifier with a 90-kHz power bandwidth. Among this amplifier's attributes is



1. THIS SIMPLE TEST circuit compares the linearity of different power op amps. The false summing node and output are connected to an X-Y display.

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an architecture that uses MOSFETs in every gain stage, with the exception of bipolar followers that drive the output MOSFET gates. This amplifier design has an open-loop distortion of about 2.5%.

Quantifying amplifier distortion under open-loop conditions is an excellent way to compare different amplifiers. This can be done by using a simple test circuit and an X-Y display *(Fig. 1)*. The summing node in the test circuit is actually a false summing node that multiplies the true noninverting input by a factor of 100. This signal is applied to the vertical axis of the X-Y display with the horizontal axis connected to the output. An oscilloscope display that compares the linearity of a bipolar (PA07) and a MOSFET (PA04) power op amp clearly favors MOSFET amplifiers for low distortion characteristics *(Fig. 2)*.

To supply low distortion and wide bandwidth, a power op amp should have the lowest possible closed-loop gain, be configured as an inverting amplifier, have external phase compensation capability, and have slew-rate-limited input signals. Distortion is directly proportional to the ratio of open-loop gain to closed-loop gain:

$$D_F = DA_F/A$$

where D_F = % distortion with feedback, D = % distortion without feedback, A = open-loop gain, and A_F = closed-loop gain.

The presence of D in the equation illustrates the importance of low open-loop distortion as an amplifier selection factor. Nevertheless, the advantage of high open-loop gain must be weighed against the resultant decrease in speed. Most power op amps are a reasonable compromise between open-loop gain and speed.

The minimum useful closed-loop gain for any application is determined by the relationship of drive available to the power op amp and its required output voltage swing. This drive often comes from a small-signal op amp with a customary output swing capability of −10 to +10 V, or 20 V_{pk-pk}. As an example, if an amplifier, such as PA04, operates at its maximum supply rails of ±100 V, a gain of 10 is required in the power op amp circuit. The low closed-loop gain approach may appear to introduce an additional source of distortion by adding this small signal op amp. However, the op amp driving the power amplifier operates at a low gain. Because it drives the power op amp's input, it's lightly loaded and contributes negligible distortion to the circuit.

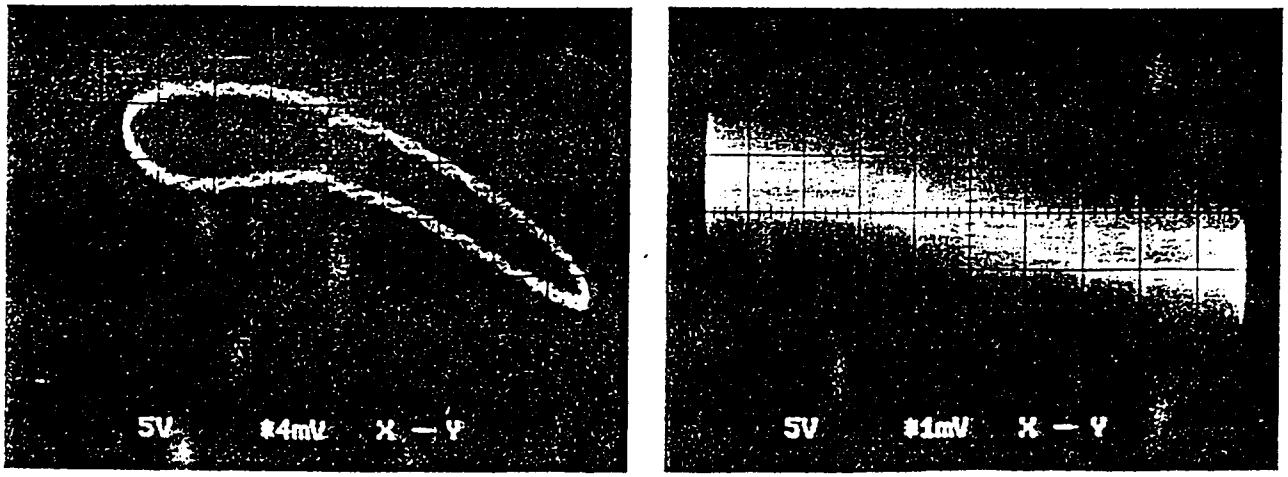
Low closed-loop gain translates to increased negative feedback, a condition which occasionally meets with unfounded objections when the requirement is low distortion. But the only problem with large amounts of negative feedback occurs under transient conditions which will be discussed later.

The inverting amplifier configuration forces common-mode potentials at the amplifier inputs to zero *(Fig. 3)*. This insures the elimination of any nonlinearity or distortion due to common-mode effects in the amplifier. The only advantages of the noninverting configuration are the lack of inversion (which may or may not be important), and greater flexibility in terms of amplifier input impedance. The noninverting configuration supplies the leeway to design for high input impedances, often into the megohm region, thus enabling the amplifier to be driven from almost any source.

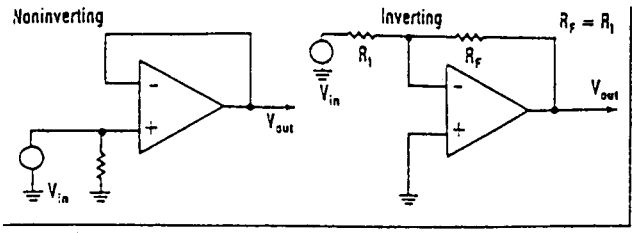
Although the inverting configuration reduces input impedance, using the two- amplifier approach for low distortion relaxes the requirements for input impedance. Furthermore, cascading two inverting amplifiers creates an overall noninverting configuration. The summing node of an inverting amplifier is also useful for sensing deviations from linear operation. Any voltage appearing at the node indicates nonlinearity, overload, or some other fault condition.

Phase Compensation

For maximum overall high-frequency performance, a power op amp should be externally phase-compensated. Because distortion is a function of loop gain, a minimum amount of external compensation is necessary to stabilize the amplifier and get the best combination of gain and bandwidth. The amplifier



2. OSCILLOSCOPE DISPLAYS of the linearity test results for the PA07 bipolar power op amp (left) and PA04 MOSFET amplifier (right) clearly favors the latter for low distortion.



3. COMMON-MODE effects differ between amplifier configurations. In the noninverting circuit, both input terminals experience large voltage swings. In the inverting mode, both inputs are always at 0 V, even when the input and output voltages are at ±10 V.

doesn't have to be stable at unity gain. Because power amplifiers usually have larger output-voltage swings than their driving circuits could normally accommodate, they must operate at a gain well above unity.

A small-signal response curve for the PA04 illustrates the advantage of using external phase compensation over compensation for unity-gain stability *(Fig. 4)*. One improvement is better open-loop bandwidth as a result of reduced phase compensation. The straight line at 20 dB is the bandwidth plot of a closed-loop amplifier with 20 dB gain. Slew rate and power bandwidth also rise accordingly. In addition, loop gain at 20 kHz is only 20 dB for unity gain compensation, while compensation for a gain of 10 produces about 28 dB of loop gain. This loop-gain increase reduces distortion by a factor of 2.5.

Low closed-loop gain in op-amp circuits results from a large amount of negative feedback, which is normally a desirable condition. But when a step function is applied to the amplifier input, the large feedback prevents the output from responding instantaneously. During the time required for the output to catch up to the input, the input experiences a large differential input *(Fig. 5)*. This causes the amplifier to enter a nonlinear or open-loop condition during this slew-rate-dependent waiting period. The resultant overload also induces a slow and poorly behaved recovery while the amplifier returns to linear operation after the slew interval.

This problem is avoided by simply restricting the rise times of input signals to fall within the amplifier's slew capability. When the source of these signals can't be controlled, a low-pass filter is required at the amplifier input to control input slew rate.

The filter time constant is based on the rated slew rate of the amplifier and the gain of the circuit, and it's selected to limit the maximum possible rate-of-change of the input signal to less than or equal to the amplifier slew rate. The maximum acceptable rate-of-change at the input is determined by dividing the amplifier slew rate by the amplifier gain. With a known maximum step function input, the maximum rate of change at the low-pass filter's output occurs at t=0 and is determined by:

$$dv/dt = (V/R)/C$$

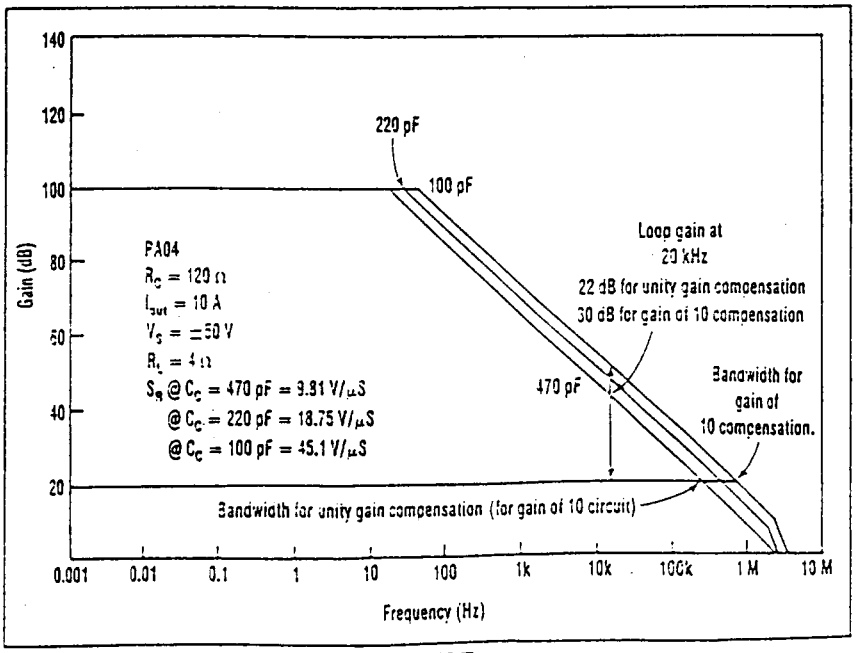
The RC time constant t_{RC} required at the amplifier input is:

$$t_{RC} = (V_{in}A_V)/S_R$$

where V_{in} = peak-to-peak input voltage, A_V = closed-loop gain, and S_R = specified amplifier slew rate.

This method of selecting component values for an input slew-rate-limiting filter only requires readily available information on amplifier data sheets. It may appear that an input filter would compromise high frequency response. However, a low-pass filter designed by this method for the PA04 with a gain of 10 has a 3 dB point at 40 kHz. This technique doesn't significantly degrade bandwidth performance as it enhances transient behavior.

When a power amplifier drives a capacitive load, the interaction between output resistance and capacitive reactance loading creates an additional pole and attendant phase shift in amplifier response *(Fig. 6)*. Inductive loads produce less obvious problems which lead to amplifier instability. Most follower type output stages are immune to the effects of inductive loads, but drain or collector output stages require local feedback loops in the output stages. These loops can cause circuit oscillation when their impedances increase at high frequencies. Several protective



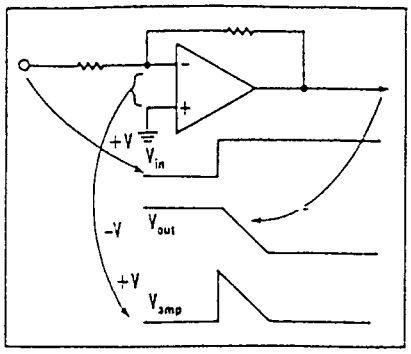
4. THE SMALL-SIGNAL RESPONSE for the PA04 exhibits improved open-loop bandwidth, power bandwidth, and slew rate resulting from external phase compensation usage instead of compensation for unity-gain stability. The improved loop gain for a gain-of-10 compensation reduces distortion by a factor of 2.5.

measures can be applied to prevent instability:

1. Add a capacitor in the feedback path to supply a compensating phase shift to counteract phase lag that's due to either amplifier response or capacitive loading *(Fig. 7a)*.
2. Add a parallel inductor-resistor combination in series with the amplifier output, plus feedback tapped from amplifier output in front of the inductor *(Fig. 7b)*. This technique isolates the effect of the capacitive loading from the amplifier response by inserting a compensating impedance in series with the amplifier output and capacitive load.
3. Connect a series resistor and capacitor between the amplifier output and ground *(Fig. 7c)*. This arrangement ensures a low resistive load on the amplifier output at high frequencies to compensate for the effects of inductive loads.
4. Place a series R-C combination across the amplifier inputs to increase noise gain and decrease feedback at high frequencies to the point where stability isn't a problem *(Fig. 7d)*.

Methods 2 and 3 offer the best overall bandwidth performance and transient behavior, and they're favored for use with wideband and low distortion designs. By contrast, the feedback capacitor mentioned in method 1 rolls off the amplifier at high frequencies, resulting in 100% feedback at these frequencies. This requires compensating amplifiers for unity gain stability, sacrificing high-frequency loop gain, and accompanying distortion reduction. It's important to use care with this technique, because it can be useful in controlling overshoots and ringing.

The noise gain compensation described in method 4 reduces the amplifier bandwidth to match that of the noise gain. To illustrate, consider an amplifier with a gain of 10, and that noise-gain compensation for a noise gain of 100 provides stability. If the bandwidth at a gain of 10 is 100 kHz, then



5. HIGH VOLTAGE LEVELS appear at the op amp input terminals during slew-rate limiting. This loading on the input stage forces the amplifier into nonlinear operation until it's recovered from the overload.

bandwidth for a gain of 100 is 10 kHz. This bandwidth will be the same for an amplifier with a gain of 10 and noise-gain compensation for a gain of 100. In addition, the amplifier response curve peaks near the high-frequency bandwidth limit of a noise-gain-compensated amplifier, and has an overshoot in the square-wave response.

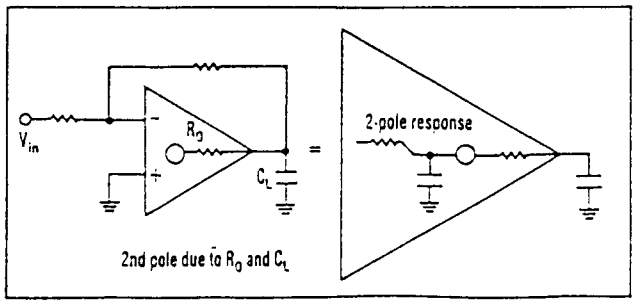
The ideal power op amp is tolerant of reactive loading. Although the PA04 is not perfect in this regard, it tolerates a capacitive loading of over 1 μF while operating at a gain of 10 with no stability problems, excessive overshoot, or ringing with square-wave inputs.

A typical state-of-the-art design for a low-distortion, wideband power op amp uses a PA04 driven by an OP37, with both in inverting-gain-of-10 configurations. The PA04's tolerance of reactive loads negates the need for additional components to ensure stability and delivers excellent bandwidth and transient performance.

With an 8-Ω load, this amplifier circuit can supply over 300 W at up to 150 kHz with the input slew-rate filter bypassed. With the filter in place, the amplifier delivers full response up to 40 kHz. Distortion never exceeds 0.02% THD. Power supplies must deliver at least 7 A to support 8-Ω loads in ac applications. Regulated supplies aren't necessary, though they're desirable from a reliability standpoint.

It's important that protective circuitry offer the required amplifier safeguards without introducing unnecessary distortion. A typical amplifier won't withstand a short circuit from output to ground. Moreover, limiting current to a safe value for this condition would severely restrict available power. However, the four-wire current-limit feature of the PA04 makes it possible to modify the basic current limit *(Fig. 8a)*. For example, assume that the low-frequency response can pass a 20-Hz square wave without distortion (this implies a low-frequency bandwidth of 2 Hz). A current-limit scheme makes this possible as it keeps the amplifier safe from short circuits to ground *(Fig. 8b)*. This circuit is a combination of foldback current-limiting (the combined effect of R_F, R_3, and R_4), and a two-pole current-limit delay (R_1, R_2, R_3, R_4, C_1, and C_2).

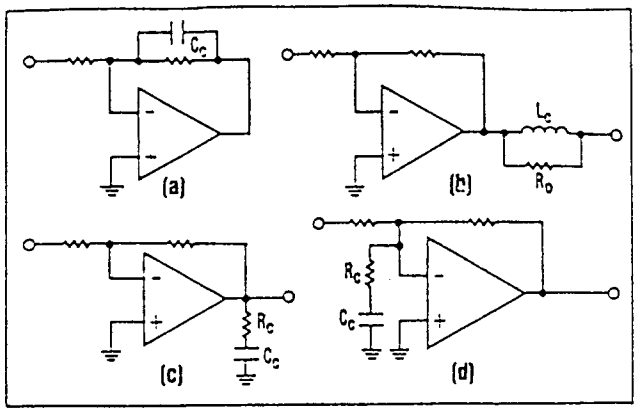
When the current limit is activated by, for example, a short circuit to ground, full current limit is delayed by the charging of the capacitors. During this time, current is limited to a value determined by R_{CL} and the foldback limit set by R_F, R3, and R4. Foldback enables the amplifier to deliver large currents when the output is close to either supply rail (current flows toward the rail closest to the output), with less current allowed as the output voltage swings farther from the rail supplying the current. Eventually, after a time long enough to keep



6. CAPACITIVE OP-AMP LOADS create an additional pole and a resultant phase shift in amplifier response, which usually means oscillation at high frequencies.

from interfering with a 20-Hz square wave, but short enough to comply with amplifier time-limited SOA (safe operating area) requirements, the current is restricted to a value low enough for a safe sustained short to ground.

Many other types of protection schemes are possible with the PA04. For example, connecting pin 12 to pin 9 disables the amplifier. Pin 12 can also be used as a control terminal for an amplifier protection circuit.



7. STABILITY-ENHANCING techniques for power op amps can counteract the effects of capacitive loading (a or b), inductive loading (c), and noise gain (d). Methods a and b deliver the best overall bandwidth performance and transient behavior.

As with any power amplifier, the PA04 requires heatsinking. Worst-case power dissipation P_D is determined by:

$$P_D = (V_S)^2/(2\pi)^2 R_L \approx (V_S)^2/20R_L$$

where V_S = rail-to-rail supply voltage and R_L = the load resistance.

In the case of Fig. 7, this value is 162 W. The heatsink should be sized to keep maximum junction temperature T_J below 150°C. For example, assuming a maximum ambient temperature T_A of 40°C, $T_R = T_J - T_A = 110$°C.

The required thermal resistance from the device junction to ambient θ_{JA} is the temperature rise divided by dissipation:

$$\theta_{JA} = 110/162 = 0.679\text{°C/W}$$

Subtracting the PA04's thermal resistance and heatsink-to-case thermal resistance yields the required thermal resistance θ_{SA} for the heatsink:

$$\theta_{SA} = \theta_{JA} - \theta_{JC} - \theta_{CS} = 0.679 - 0.4 - 0.1 = 0.179\text{°C/W}$$

This value of thermal resistance will require a substantial heatsink, probably with at least forced-air cooling. However, worst-case dissipation is unlikely to occur under normal conditions. The calculations are based on maximum values from the PA04 data sheet—the typical value for PA04 thermal resistance is 0.3°C/W.

Bipolar power op amps cost less than MOSFET types, but at the expense of compromises in bandwidth, distortion, and SOA. MOSFETs are more tolerant of stress because they're a power-limited device with no secondary breakdown region. The open-loop distortion of a MOSFET-based design is lower because of its more linear transfer function.

Bipolar power op amps should be considered carefully before they're chosen, based on low distortion or wide bandwidth. Besides open-loop tests, all of the parts should be tested over a range of load conditions at low and high signal levels (some Class A/B amplifiers exhibit a notch in their transfer function similar to crossover distortion). An excellent closed loop test is in a gain-of-100 circuit at 10 kHz, because this high gain and frequency will unmask sources of distortion that aren't obvious at lower frequencies and gains. Architectures of monolithic power op amps are all compromised with respect to stability, principally resulting from non-complementary (npn only) output stages.□

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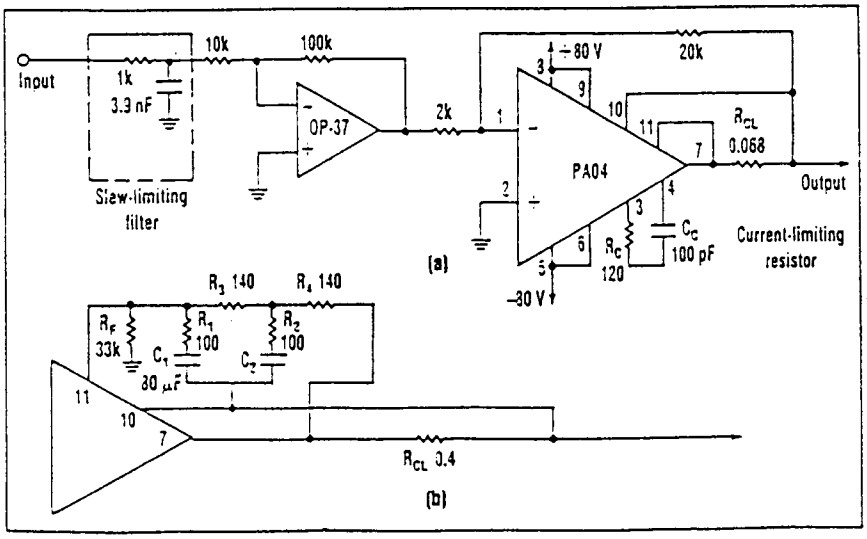

8. A HIGH-PERFORMANCE OP-AMP DESIGN uses an inverting PA04 MOSFET op amp driven by a second op amp with a slew-limiting filter at the input (a). For added protection against an output short to ground, current-limit resistor R_{CL} can be augmented by a 2-pole current-limit circuit with foldback (b).