

Applying The Super Power PA03

INTRODUCTION

The super power PA03 is the result of a design effort to substantially increase output power without sacrificing the high performance engineers are accustomed to when using small signal op amps. Thus, this new building block can perform accurate and complex tasks previously reserved to modular and rack mount devices.

The major applications for the PA03 will be in single ended circuits where up to 1,000W must be delivered to the load or in bridge motor servo systems delivering up to 2,000W peak. Linear motion control, magnetic deflection, programmable power supplies, and power transducer drives are typical of these applications. High power sonar, such as phased array, is another key application made possible by the accurate phase response and linearity of the class A/B output stage. Robot, motion control, and other high current applications which were previously impossible to implement with IC Power Op Amps because of power limits, are now possible using the PA03 as a building block.

The most powerful TO-3 hybrid IC's currently available can dissipate up to 125W and drive loads up to 250W (Apex Microtechnology PA12), while available monolithic IC's handle less. Where peak power requirements for dynamic motor control exceed 250W, three approaches were commonly used to increase power output: (1) parallel or bridge operation of two or more power op amps; (2) external booster transistors; (3) modular or rack mount power op amps.

While these options extend power capabilities, they can

have major drawbacks in increased cost, excessive weight and reduced reliability. Furthermore, the large size can be a cumbersome design burden. System designers need a small, reliable power op amp capable of producing up to 1,000W while maintaining top notch performance. The PA03 meets this challenge!

Using the super power PA03 offers many advantages. With an internal power dissipation of up to 500W, the PA03's ratings top the previously most powerful op amp (Apex Microtechnology PA12) by a factor of four, and one PA03 is more cost effective and far more reliable than four less powerful op amps. Its thermal tracking of internal bias components makes the PA03 much safer to use under abnormal conditions than several units in parallel. Moreover, internal protection circuits insure that almost any power level not violating the 2,400W, 1ms Safe Operating Area (SOA) is safe. The amplifier will shut down upon overload, avoiding self-destruction. Internal current limiting resistors eliminate bulky, expensive milliohm external resistors which are normally required for power op amps. The common collector complementary output stage allows the output to swing within 4V of the supply rail at 12A and within 6V at 30A and has full shut-down control. This gives the designer a tool to protect sensitive loads or to minimize power consumption under battery operation. By operating in class A/B, it exhibits low crossover distortion, a feature hard to implement without the inherent thermal tracking of single package construction.

An external balance control option allows the already low

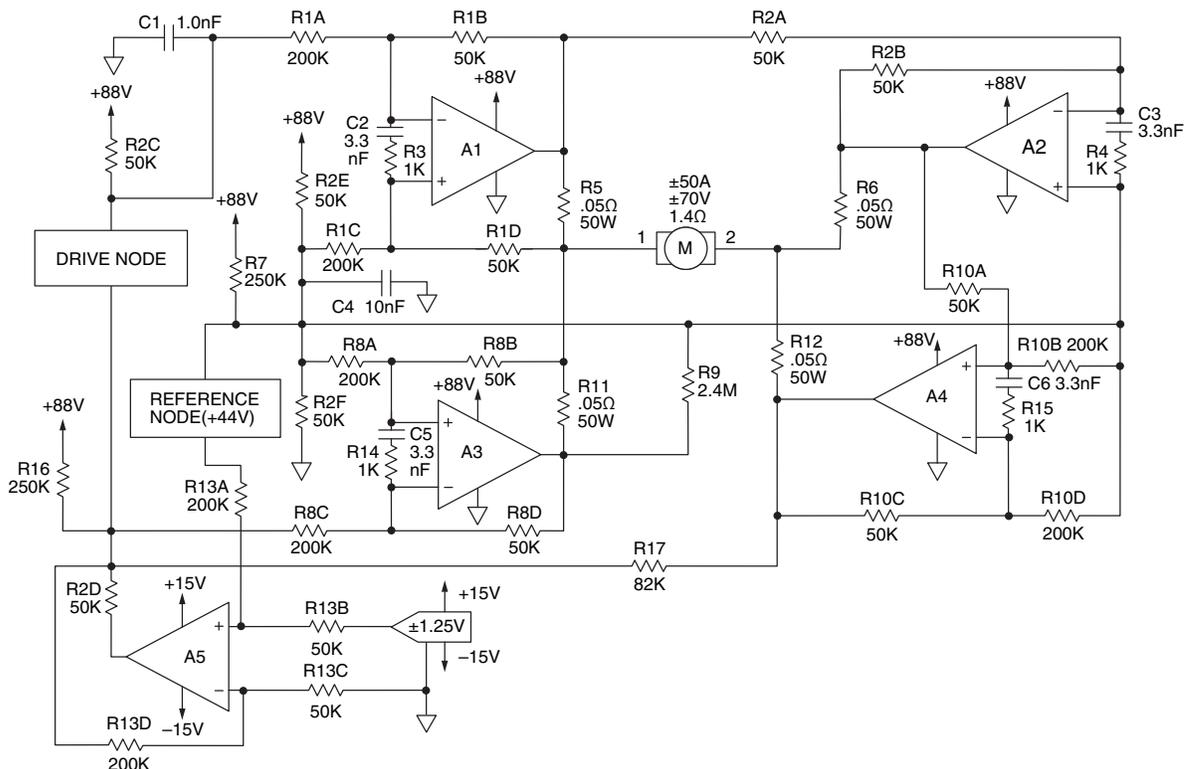


FIGURE 1. APPLYING THE SUPER POWER PA03

offset voltage to be zeroed. The PA03's high overall accuracy makes it suitable for interfacing directly to photo-diodes; to build long time period integrators; or to design 12 bit and better resolution programmable power supplies.

The super power PA03 is a hybrid IC housed in the innovative Power-Dip dual in-line package. It has .060 pins on .200 centers to accommodate higher currents and allows layout on the standard 0.100 grid. The Power-Dip copper header of the PA03 provides 8.5 times the thermal conductivity, and three times the area of the conventional steel TO-3 package.

A SUPER POWER TORQUE DRIVE

The parallel bridge circuit in Figure 1 is shown to demonstrate several possible power enhancement techniques in one application. It operates in the transimpedance mode to drive the torque motor. This allows the D to A converter (DAC) to be programmed directly for delivered torque, since motor torque is directly proportional to armature current. The bridge uses an economic and efficient single output power supply and doubles delivered power levels again by increasing the current drive capability. Delete A3 and A4, and associated components if this option is not required.

Looking at the bridge configuration first, A2 and A4 invert the output of A1 and A3 with respect to the mid-supply reference node. Therefore, A2 and A4 drive the load equal to A1 and A3 in the opposite direction about the mid-supply reference point. The mid-supply node assures that neither amplifier saturates prematurely. Figure 2 shows the actual output voltages of A1/A3 and A2/A4 when delivering full scale output currents to the torque motor.

A5 (Figure 1) configured as a level shifter at a gain of 4,

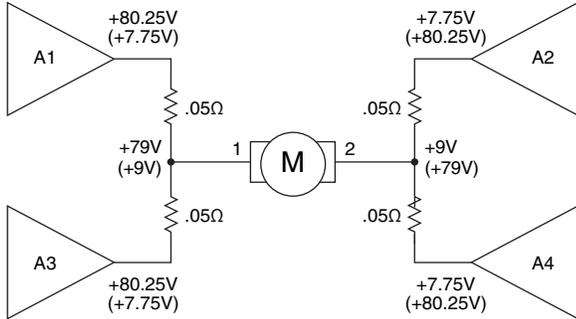


FIGURE 2. FULL SCALE DRIVE VOLTAGES

takes the 1.25V input from the DAC and swings the drive node to $\pm 5V$ with respect to the reference node. A1 and A3 each amplify this differential 5V signal to a $\pm 25A$ output level driving terminal 1 of the motor. A4 is a unity gain follower of the A2 output voltage. Since A2 and A4 have equal output voltages and equal current control resistors, they share the total 50A current equally.

The very low bias current of the PA03 FET input stage makes it possible to keep power dissipation low by using relatively large value precision resistors. This not only minimizes temperature variations in the resistive networks, but also reduces power dissipation in A5. Current balancing for both the reference and drive nodes is used to prevent level shifting of the high impedance nodes as a function of drive voltage. This is an easy task because of the symmetric drive levels with respect to the reference node.

Figure 3 shows a breakdown of the currents associated with

the reference node. R2E and R2F form the basic voltage divider. At a zero drive level, the current through R13A and R13B will match the current through R7. The voltages applied to R1, R8, R9, and R10 will all be zero with respect to the 44V reference so the circuit is balanced. The voltages shown correspond to full scale drive level. R7 roughly balances the current through R13A and R13B to the +1.25V DAC input. R10A, R10B, R10C, and R10D current will nearly match the currents of R1C and R1D plus R8A and R8B. The differences encountered so far total 15 microamps, which is provided by R9 to insure the reference node remains at 44V.

Figure 4 illustrates currents associated with the drive node

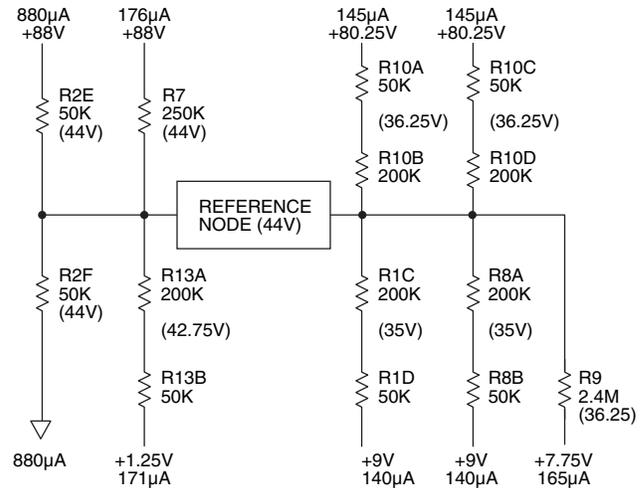


FIGURE 3. CURRENT BALANCING OF THE REFERENCE NODE

where R2C and R2D form the basic voltage divider. At zero drive, no voltage is applied to R17, R1 and R8, and the output of A5 will be zero and the drive node voltage will be 44 volts. This means currents of R2C and R2D balance. The currents in R16 balance the currents of R13C and R13D and the remaining resistor currents are zero. For a full scale input of +1.25V, A5 will drive to approximately +10V. The currents through R16, R13C and R13D are no longer balanced because the drive node voltage has risen to 49V. The currents through R1A and R1B, plus R8C and R8D, make the node even less balanced. R17 was selected to slightly over compensate the current imbalance. Since the differential circuit of A5 (Figure 1) controls drive node voltage, its nominal swing will be a 9.44V,

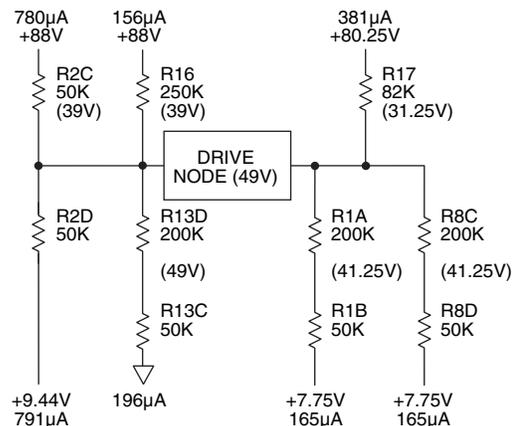


FIGURE 4. CURRENT BALANCING OF THE DRIVE NODE

time of 4s, the power dissipation is only the quiescent power of 9.8W. This means the average power dissipated is only 41.9W. With a heatsink that has a thermal time constant of ten seconds, the highest peak (306W for 500ms) amounts to 5% of the time constant, or 4.9% of the rise for 306W continuously. Adding this spike equivalent of 15W to the 41.9W average will bring the peak short term equivalent power to 57.23W (though this peak could vary slightly depending upon the exact timing).

If, for reliability, a peak junction temperature of 150°C is selected, and a maximum ambient temperature of 38°C is assumed, the allowable temperature rise of the heatsink is 18°C (150°C– 38°C– 92°C). At a peak short term equivalent of 52.2W, this requires a heatsink rated at 0.35°C/W. The Apex Microtechnology HS06 (0.6°C/W free air) with a forced air velocity of 500 ft/min can provide the required rating.

In this application, if abnormal situations arise due to faulty timing or defective test units, short term operation at the 306W level will not destroy the PA03 because the thermal shutdown will limit the temperature rise. The worst case would be a short in the test socket which could push the PA03 to a maximum current limit of 42A. At this current, the sense resistor (R_S) would drop 2.1V leaving 36.9V across the PA03. These current and voltage levels (1.55KW) are well within the PA03's 1ms second breakdown line of the SOA curve. Therefore, the fast response of the PA03's thermal shutdown circuit will protect the power op amp for the time required to eliminate the short.

REMOTE SITE MOON BOUNCE ANTENNA MOTOR DRIVE

Power conservation is essential for solar powered data gathering, while a considerable amount of motive force is required for positioning a 40 Ft dish antenna.

With a 3° beam angle and a position accuracy of 0.5°, the lunar angular velocity of 14.4°/Hr allows a position update only once per minute. The PA03's shutdown control used for intermittent operation combined with a worm gear drive to hold position during shutdown periods, facilitates an energy efficient positioning system.

The D to A Converter in Figure 7 converts position data to a voltage which is fed to the inverting input of the PA03 configured as an integrator by feedback capacitor C1 and input resistor R1. The precision reference and potentiometer apply a feedback voltage equivalent to actual position to the non-inverting input. The PA03 drives the motor with the integrated difference between the desired and actual positions. R2 acts as a damping element limiting the integration time constant

to minimize overshoot.

The shutdown control is released for six seconds after each position update, which allows the PA03 sufficient time to position the antenna and reduces the standby power to 2W for 54 seconds or 90% of the time.

The normal current requirement of the motor is 8A, but under high wind conditions, up to 17A may be drawn. In this application, the amplifier output will be decaying pulse; thus driving the motor to a new position once a minute. Because the amplifier is at maximum output (saturated) most of the time, the power dissipation at the full output voltage is the appropriate level to calculate.

At 17A the PA03 will drive to within 5.5V of the supply voltage (rail) dissipation of 93.5W. The quiescent current of 0.2A times the total supply voltage of 48V adds another 9.6W for a total of 103.1W dissipated in the amplifier. At the maximum ambient temperature of 45°C and a maximum junction temperature of 140°C, the allowable rise is 95°, which requires a thermal resistance for the heatsink as follows:

$$Q_{HS} = 95/103.1 - 0.3 = 0.62^{\circ}\text{C/W}$$

The Apex Microtechnology HS06 meets this criteria.

Under normal low wind conditions, the peak battery drain will be 201.6W. However, due to the 10% maximum duty cycle and the power-saving shutdown feature of the PA03, the average power consumption will be only:

$$P_{AV} = 0.1 (24 \cdot 8 + 48 \cdot 0.2) + 0.9 (48 \cdot 0.040) = 22\text{W}$$

To further reduce standby power to 2W, the shutdown feature can be activated only when communications are required.

USING THE PA03 IN YOUR APPLICATION

To achieve maximum efficiency, the power supply voltage should be selected for the minimum voltage necessary to produce the required output.

For example, to obtain a ±45V output at 12A, add the supply-to-output differential as specified on the Data Sheet (±5V) to produce ±50V.

Dual supplies may be as high as ±75V and asymmetric or single supply operation is permitted as long as the total rail-to-rail voltage doesn't exceed 150V. Input voltages must always be at least 10V less than the power supply voltage due to the common mode voltage specification being supply voltage minus 10V.

Because of the greater power levels involved, the thermal path to remove the heat from the amplifier is of great importance to the successful application of the PA03. A 1°C/W rated heatsink may be suitable to remove 20-50W, but it is insufficient to handle 500W. For the PA03, a heatsink with a thermal resistance on the order of 0.1°C/W is often required such as: very large surfaces, forced air cooling, or even water cooling. Fortunately, if insufficient heatsinking is provided, the unique safety circuits of the PA03 will generally result in thermal shutdown rather than destruction. Destructive power levels are so high that in most applications they need not be of any concern.

As with all high current Power Op Amps, precautions must be taken to avoid current feedback due to voltage drops in the wiring of electromagnetic radiation. This is especially true when using the PA03 because of its higher current rating. The wiring for all supply and output leads must be done with wire equivalent to 12 gauge or thicker, as the PA03 has a higher current capacity than most branch circuits in residential wiring.

To avoid feedback through the power supplies, they must be bypassed with a ceramic capacitor of 0.47µF or greater,

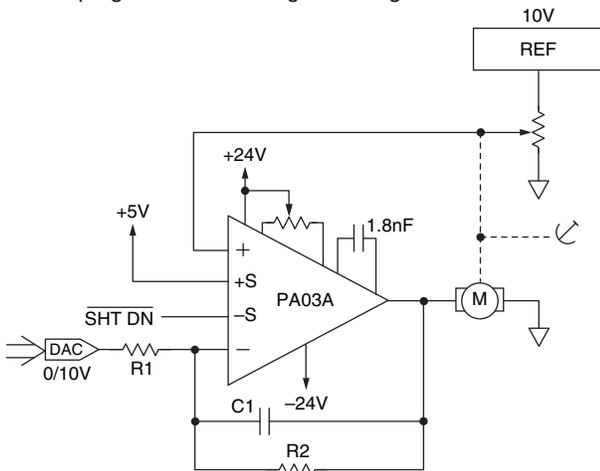


FIGURE 7. REMOTE SITE MOON BOUNCE APPLICATION

in parallel with a 10μF per ampere of peak output current (up to 300μF), mounted not more than 1.5 inches from the supply lines.

Even when using excellent bypassing components, good layout techniques and quality power supplies can easily cause substantial AC ripple. Ripple must be considered as a possible source of error. Positive feedback can also occur if the power supply also powers other circuit elements.

WATCH THE POWER DISSIPATION

The internal power dissipation (P) in a DC circuit is:

$$P = (V_s - V_o) I_o + (I + V_s I + I - V_s I) I_q$$

where: I_o : OUTPUT CURRENT
 I_q : QUIESCENT CURRENT
 V_o : OUTPUT VOLTAGE
 V_s : SUPPLY VOLTAGE

Errors often arise in the calculation if the wrong supply voltage is used. The voltage (V_s) must be the one at the supply pin sinking or sourcing the current. Incorrect selection of the worst case conditions (short to ground or supplies) can also create errors.

When driving reactive loads, due to the phase shift between output voltage and current, the power dissipation may be several times higher than the equivalent resistive loads. These have a totally different, but equally simple approach that can be used to obtain the correct power dissipation (P):

$$P = P_i - P_o$$

where: P_i = POWER DRAWN FROM THE POWER SUPPLY
 P_o = POWER DELIVERED TO THE LOAD

Keep in mind that using purely reactive loads means that all power drawn from the supplies is dissipated in the amplifier.

JUNCTION TEMPERATURES

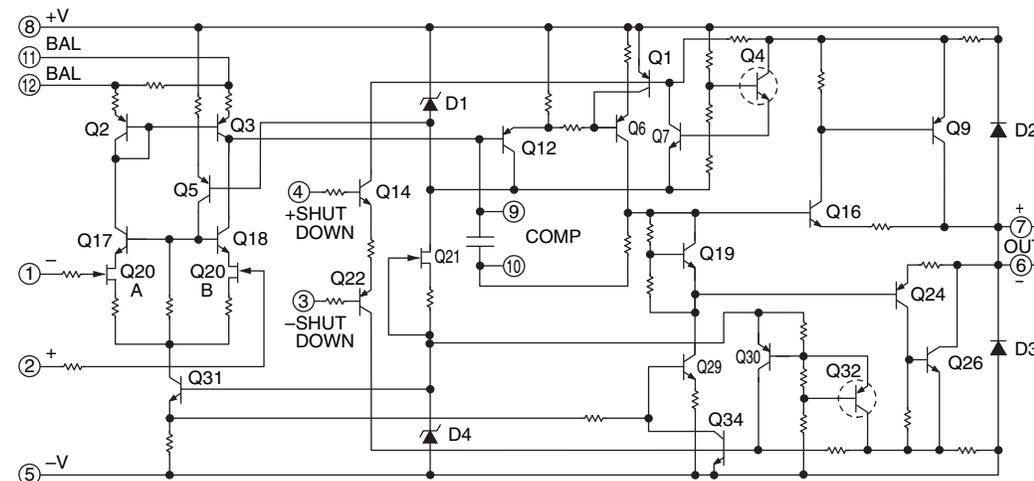


FIGURE 8. PA03 EQUIVALENT SCHEMATIC

The absolute maximum power dissipation of the PA03 is 500W and was derived using the industry standard derating procedure. This assumes operation at maximum junction temperatures (175°C) with the case at 25°C.

With the power dissipation and the maximum ambient temperature (T_A) of the application known, the operating temperatures of both case (T_C) and junction (T_J) of the power transistors can be determined:

$$T_C = T_A + P \cdot \Theta_{HS}$$

where: Θ_{HS} = THERMAL RESISTANCE FROM THE HEAT-SINK MOUNTING SURFACE TO AMBIENT AIR

Θ_{JS} = INTERNAL THERMAL RESISTANCE, JUNCTION TO CASE

Apply this to the PA03 by following these steps:

1. Calculate the maximum internal power dissipation (P).
2. Determine the maximum junction temperature allowable to achieve the desired reliability of the PA03. This must be less than 175°C. Apex Microtechnology recommends 150°C or less.
3. Calculate $T_J - T_A$, the allowable rise of the junction temperature above the maximum ambient temperature.
4. Calculate the required thermal resistance of the heatsink:

$$\Theta_{HS} = (T_J - T_A) / P - \Theta_{JC}$$

For example, in a circuit dissipating 300W at an ambient temperature of 30°C and the junction temperature not to exceed 150°C:

$$\Theta_{HS} = (150 - 30) / 300 - 0.3 = 0.1^\circ\text{C/W}$$

HOW THE PA03 WORKS

The circuit diagram shown in Figure 8 shows that the input section of the PA03 is similar to most Apex Microtechnology FET input hybrid power op amps. Q21, D1 and D4 form voltage references to bias both input and output stages of the amplifier. Q31 is the current source for the input stage which consists of Q20A and Q20B (the FET input pair), Q17 and Q18 (the cascode transistors), and Q2 and Q3 (the half dynamic load). The current through Q5 sets the operating voltage (source-drain) for the FET input pair. Q12 acts as an impedance buffer between the high output impedance of the input stage and Q6, the output driver.

The collector load of output driver Q6 consists of current source, Q29, and the output stage consisting of Q16, Q9, Q24, and Q26. The common collector configuration of Q9 and Q26 enable the PA03 output to swing close to the supply rails. Inverters Q16 and Q24, form local feedback networks which cause the output stage to be linear like an emitter follower with very high input impedance. The V_{BE} multiplier Q19, provides DC bias for the output transistors via Q16 and Q24, and is thermally

coupled to the power dissipating transistors in the output stage. In addition, the V_{BE} multiplier utilizes thermistors to fine tune the temperature stability of the quiescent current through output transistors Q9 and Q26. This class A/B stage provides low crossover distortion, as well as stability of the quiescent current over the full temperature range.

D2 and D3 are high speed diodes which protect the output

AN06

stage from inductive kickback by bypassing it into the supply rails. The 18.6 milliohm emitter resistors of Q9 and Q26 sense the output current of the amplifier. Currents in excess of 35 amps will develop .65 volts, thereby turning on Q1 or Q34. In turn, these transistors rob the base drive from Q6 or Q29, thus limiting the output currents to 35A. Q4 and Q32 are the sensors for the innovative SOA protection of the PA03. These two transistors are mounted directly on top of power transistors Q9 and Q26, eliminating thermal gradients and minimizing the response time to temperature changes in the output transistor junctions. The emitters of the sensors are connected to Q7 and Q30 which act as level translators to turn on current limit transistors Q1 and Q34, respectively. The complementary pair Q14 and Q22 activate the shut down of the PA03. While common mode voltage is rejected, differential voltages applied between these two transistors turn on the current limit circuit consisting of Q1 and Q34, thereby shutting down the entire output stage. In this mode the output pins appear as a high impedance to the load. Figure 9 illustrates the physical arrangements to achieve fast and reliable thermal shut down.

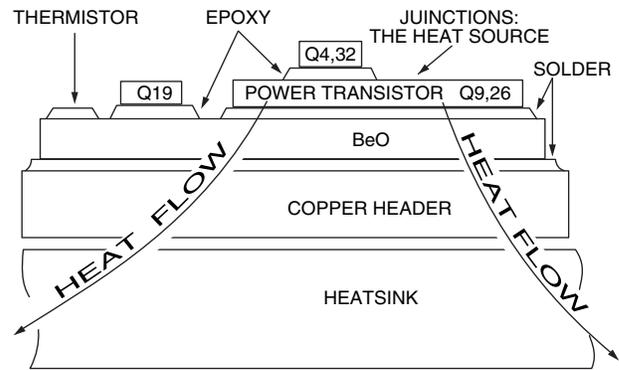


FIGURE 9. THERMO-MECHANICAL DESIGN

CONCLUSION

The PA03 is a versatile new building block which eases many design tasks and overcomes size and weight barriers which previously prevented implementation of linear power controls in limited space. The giant step up in power levels, improved protection circuits and high performance small signal characteristics make the PA03 a very cost effective innovation.

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