

## *Power Operational Amplifier*



### FEATURES

- Gain Bandwidth Product — 4 MHz
- Temperature Range —  $-55$  to  $+125^{\circ}\text{C}$  (PA10A)
- Excellent Linearity — Class A/B Output
- Wide Supply Range —  $\pm 10\text{V}$  to  $\pm 50\text{V}$
- High Output Current —  $\pm 5\text{A}$  Peak



### APPLICATIONS

- Motor, Valve and Actuator Control
- Magnetic Deflection Circuits up to 4A
- Power Transducers up to 100 kHz
- Temperature Control up to 180W
- Programmable Power Supplies up to 90V
- Audio Amplifiers up to 60W RMS

### DESCRIPTION

The PA10 and PA10A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

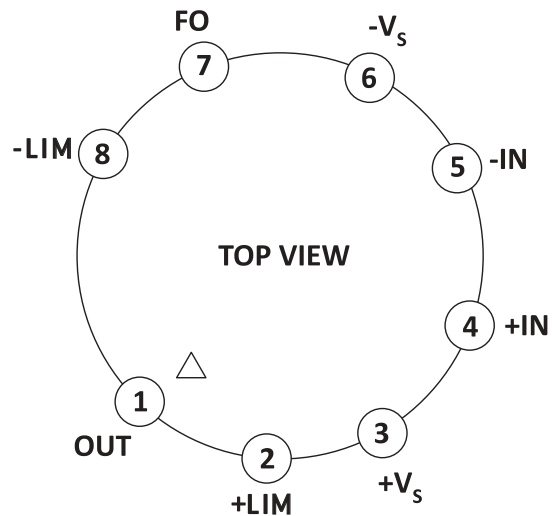
This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

The circuit diagram shows a 12-bit DAC implemented with an op-amp (A1) and a ladder network. The op-amp is configured as a voltage follower, with its non-inverting input (+) connected to the output (6) and its inverting input (-) connected to the output of the ladder network. The ladder network consists of a series of resistors and transistors (Q1, Q4, Q3, Q5, Q2A, Q2B, Q6A, Q6B) that convert the 12-bit digital input (3, 4, 5, 6) into an analog output (1, 2, 7, 8). The output is taken from the op-amp's output (6) and is connected to the output terminal (1). The circuit is powered by a 12V supply (3) and a ground (6). The op-amp is labeled A1 and the capacitor is labeled C1.

The diagram shows a PA10 operational amplifier configured as a voltage follower. The non-inverting input (+) is connected to the output (OUT) through a feedback resistor  $R_f$ . The inverting input (-) is connected to the input signal through a resistor  $R_i$ . The op-amp is powered by a positive supply  $+V_S$  and a negative supply  $-V_S$ . Input clamping diodes  $R_{LIM+}$  and  $R_{LIM-}$  are connected between the input and the respective supply rails. The output is connected to a load resistor  $R_L$ . The op-amp is labeled PA10 and has pins for  $+V_S$ ,  $-V_S$ ,  $FO$ , and  $OUT$ . The input signal is represented by an AC source symbol.

## PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	OUT	The output. Connect this pin to load and to the feedback resistors.
2	+LIM	Connect to the current limit resistor. Output current flows into/out of these pins through $R_{LIM}$ . The output pin and the load are connected to the other side of $R_{LIM+}$ .
3	+V <sub>S</sub>	The positive supply rail.
4	+IN	The non-inverting input.
5	-IN	The inverting input.
6	-V <sub>S</sub>	The negative supply rail.
7	FO	The foldover current limit. Connect to ground if desired. See “Current Limiting” section.
8	-LIM	Connect to the current limit resistor. Output current flows into/out of these pins through $R_{LIM}$ . The output pin and the load are connected to the other side of $R_{LIM-}$ .

## SPECIFICATIONS

The power supply voltage for all tests is  $\pm 40\text{V}$ , unless otherwise noted as a test condition. Full temperature range specifications are guaranteed but not tested.

### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_S$ to $-V_S$		100	V
Output Current, within SOA	$I_{OUT}$		5	A
Power Dissipation, internal	$P_D$		67	W
Input Voltage, differential	$V_{IN(Diff)}$		$\pm 37$	V
Input Voltage, common mode	$V_{CM}$		$\pm V_S$	$V_S$
Temperature, pin solder, 10s max.			350	$^{\circ}\text{C}$
Temperature, junction <sup>1</sup>	$T_J$		200	$^{\circ}\text{C}$
Temperature Range, storage		-65	+150	$^{\circ}\text{C}$
Operating Temperature Range, case	$T_C$	-55	+125	$^{\circ}\text{C}$

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

### CAUTION

The internal substrate contains beryllia ( $\text{BeO}$ ). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of  $850^{\circ}\text{C}$  to avoid generating toxic fumes.

**INPUT**

Parameter	Test Conditions	PA10			PA10A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial	$T_C = 25^\circ\text{C}$		$\pm 2$	$\pm 6$		$\pm 1$	$\pm 4$	mV
Offset Voltage vs. temperature	Full temp range		$\pm 10$	$\pm 65$		*	$\pm 40$	$\mu\text{V}/^\circ\text{C}$
Offset Voltage vs. supply	$T_C = 25^\circ\text{C}$		$\pm 30$	$\pm 200$		*	*	$\mu\text{V}/\text{V}$
Offset Voltage vs. power	$T_C = 25^\circ\text{C}$		$\pm 20$			*		$\mu\text{V}/\text{W}$
Bias Current, initial	$T_C = 25^\circ\text{C}$		12	30		10	20	nA
Bias Current vs. temperature	Full temp range		$\pm 50$	$\pm 500$		*	*	$\text{pA}/^\circ\text{C}$
Bias Current vs. supply	$T_C = 25^\circ\text{C}$		$\pm 0.10$			*		$\text{pA}/\text{V}$
Offset Current, initial	$T_C = 25^\circ\text{C}$		$\pm 12$	$\pm 30$		$\pm 5$	$\pm 10$	nA
Offset Current vs. temperature	Full temp range		$\pm 50$			*		$\text{pA}/^\circ\text{C}$
Input Impedance, DC	$T_C = 25^\circ\text{C}$		200			*		M $\Omega$
Input Capacitance	$T_C = 25^\circ\text{C}$		3			*		pF
Common Mode Voltage Range <sup>1</sup>	Full temp range	$\pm V_S - 5$	$\pm V_S - 3$		*	*		V
Common Mode Rejection, DC <sup>1</sup>	Full temp range, $V_{CM} = \pm V_S - 6\text{V}$	74	100		*	*		dB

1.  $+V_S$  and  $-V_S$  denote the positive and negative supply rail respectively. Total  $V_S$  is measured from  $+V_S$  to  $-V_S$ .

**GAIN**

Parameter	Test Conditions	PA10			PA10A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop Gain @ 10 Hz	$T_C = 25^\circ\text{C}$ , 1 k $\Omega$ load		110			*		dB
Open Loop Gain @ 10 Hz	Full temp range, 15 $\Omega$ load	96	108		*	*		dB
Gain Bandwidth Product @ 1 MHz	$T_C = 25^\circ\text{C}$ , 15 $\Omega$ load		4			*		MHz
Power Bandwidth	$T_C = 25^\circ\text{C}$ , 15 $\Omega$ load	10	15		*	*		kHz
Phase Margin	Full temp range, 15 $\Omega$ load		35			*		°

## OUTPUT

Parameter	Test Conditions	PA10			PA10A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing <sup>1</sup>	T <sub>C</sub> =25°C, I <sub>OUT</sub> =5A	±V <sub>S</sub> - 8	±V <sub>S</sub> - 5		±V <sub>S</sub> - 6	*		V
Voltage Swing <sup>1</sup>	Full temp range, I <sub>OUT</sub> = 2A	±V <sub>S</sub> - 6			*			V
Voltage Swing <sup>1</sup>	Full temp range, I <sub>OUT</sub> = 80mA	±V <sub>S</sub> - 5			*			V
Current, peak	T <sub>C</sub> = 25°C	5			*			A
Settling Time to 0.1%	T <sub>C</sub> =25°C, 2V step		2			*		μs
Slew Rate	T <sub>C</sub> = 25°C	2	3		*	*		V/μs
Capacitive Load	Full temp range, A <sub>V</sub> = 1			0.68			*	nF
Capacitive Load	Full temp range, A <sub>V</sub> = 2.5			10			*	nF
Capacitive Load	Full temp range, A <sub>V</sub> > 10			SOA			*	

1. +V<sub>S</sub> and -V<sub>S</sub> denote the positive and negative supply rail respectively. Total V<sub>S</sub> is measured from +V<sub>S</sub> to -V<sub>S</sub>.

## POWER SUPPLY

Parameter	Test Conditions	PA10			PA10A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage	Full temp range	±10	±40	±45	*	*	±50	V
Current, quiescent	T <sub>C</sub> = 25°C	8	15	30	*	*	*	mA

## THERMAL

Parameter	Test Conditions	PA10			PA10A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case <sup>1</sup>	T <sub>C</sub> =-55 to 125°C, F > 60 Hz		1.9	2.1		*	*	°C/W
Resistance, DC, junction to case	T <sub>C</sub> = -55 to 125°C		2.4	2.6		*	*	°C/W
Resistance, junction to air	T <sub>C</sub> = -55 to 125°C		30			*		°C/W
Temperature Range, case	Meets full range specs	-25		+85	-55		+125	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

**Note:** \*The specification of PA10A is identical to the specification for PA10 in applicable column to the left.

## TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

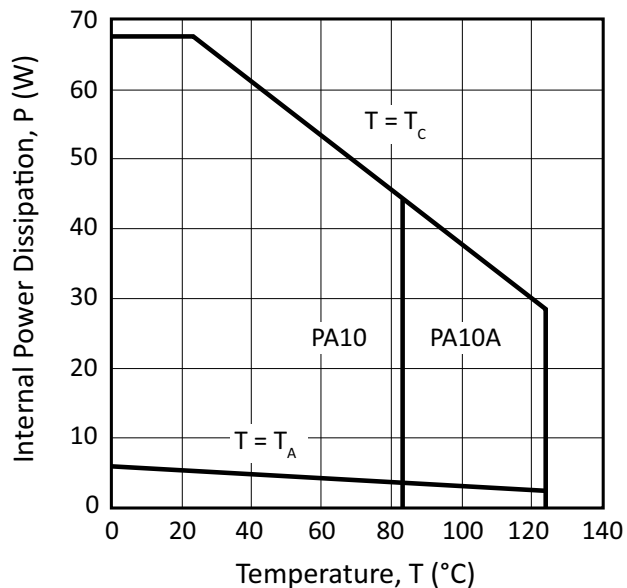


Figure 5: Bias Current

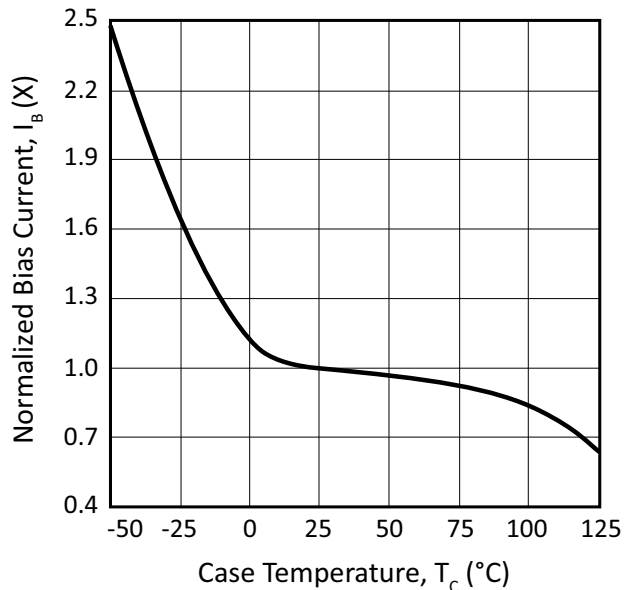


Figure 6: Small Signal Response

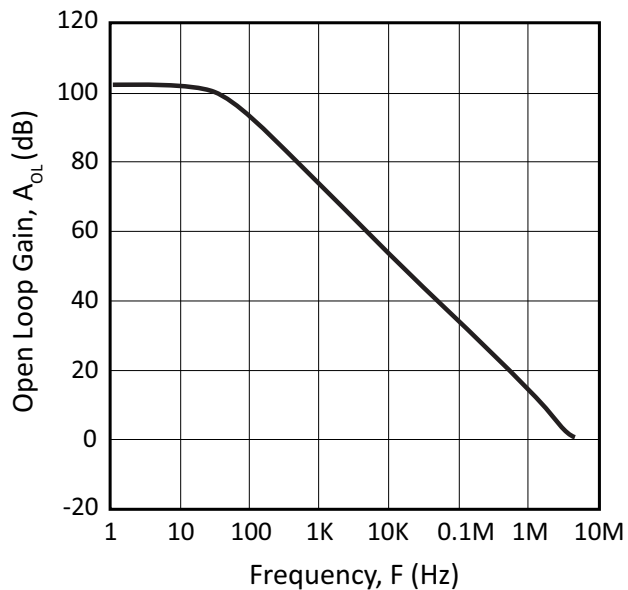


Figure 7: Phase Response

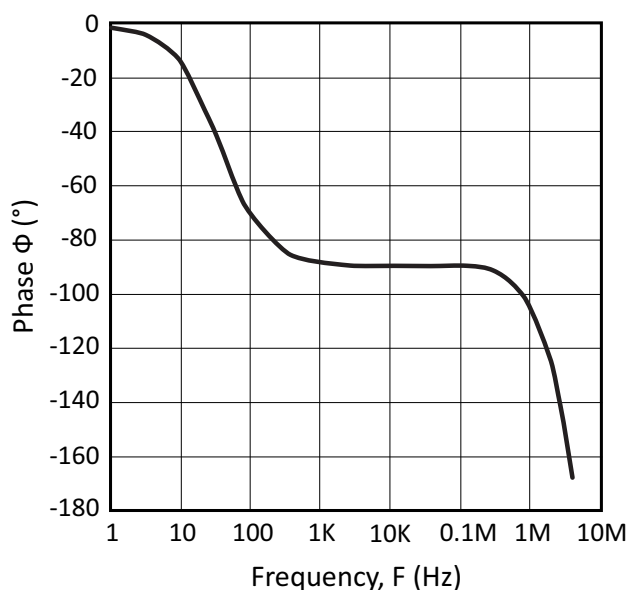


Figure 8: Current Limit

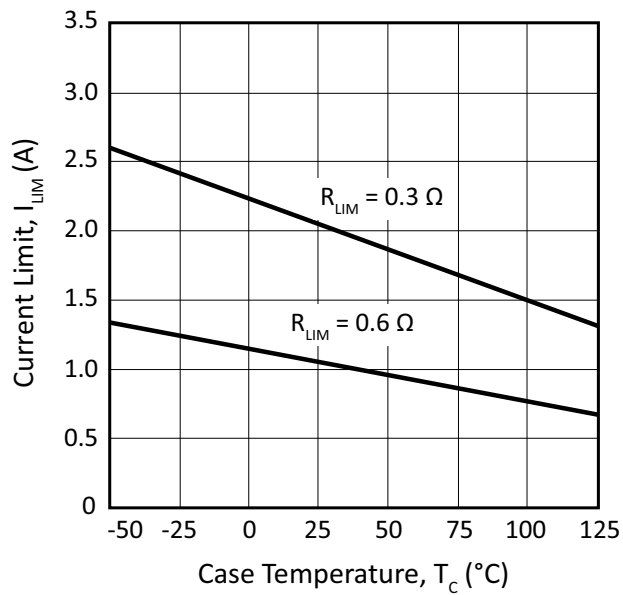


Figure 9: Power Response

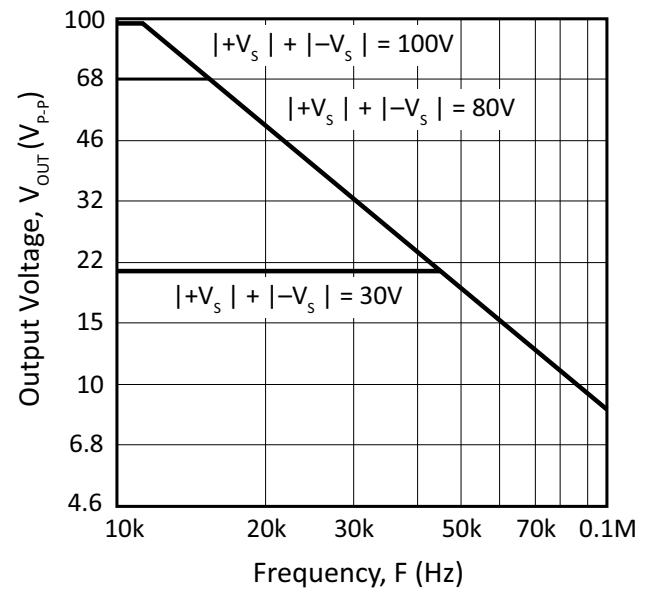


Figure 10: Common Mode Rejection

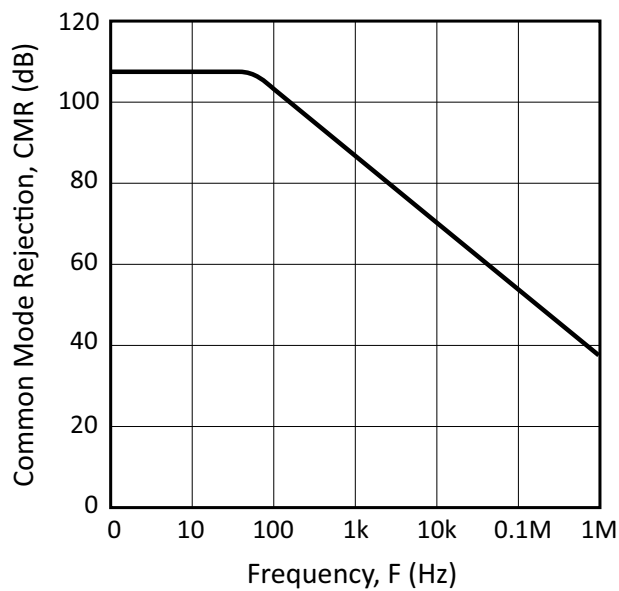


Figure 11: Pulse Response

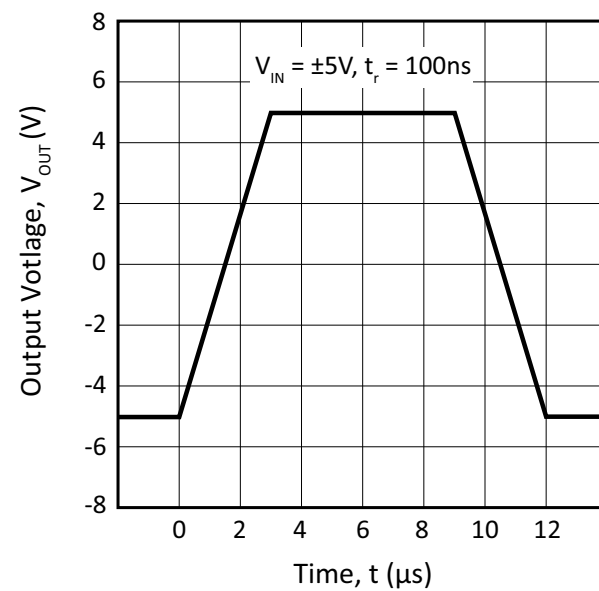




Figure 12: Input Noise

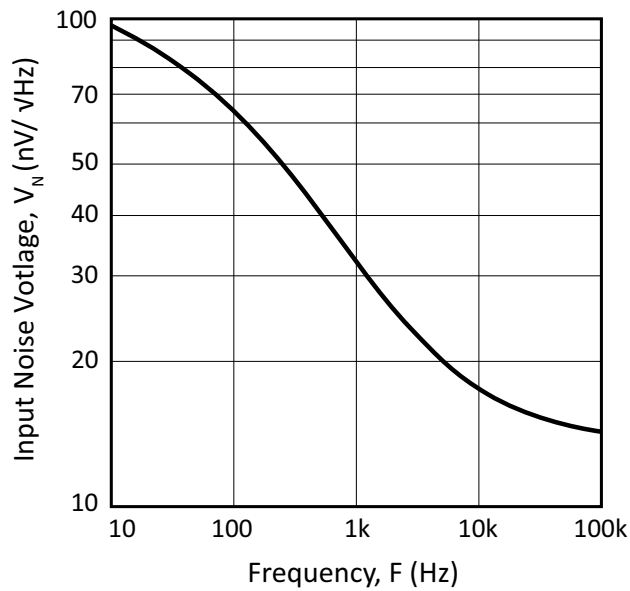


Figure 13: Harmonic Distortion

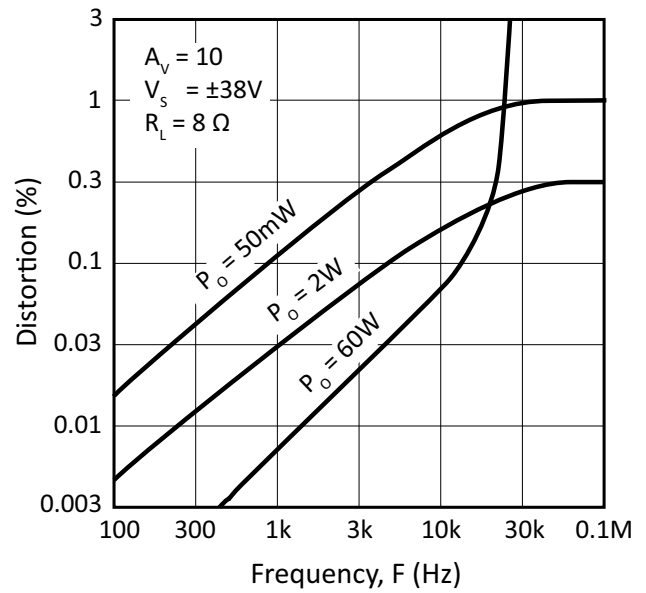


Figure 14: Quiescent Current

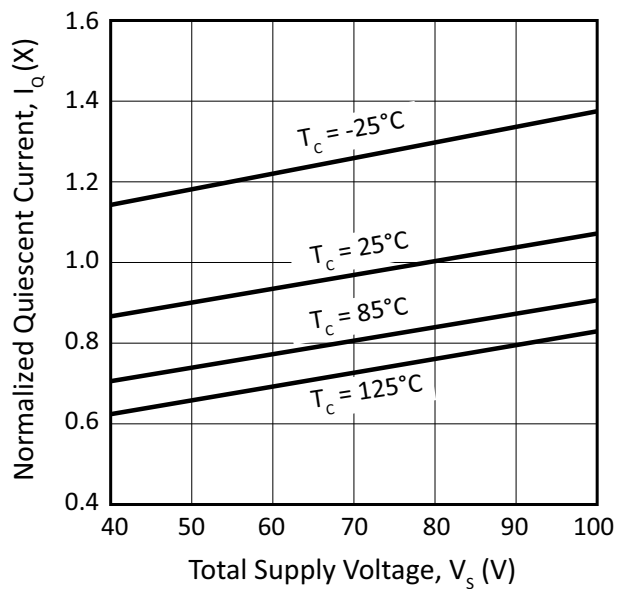
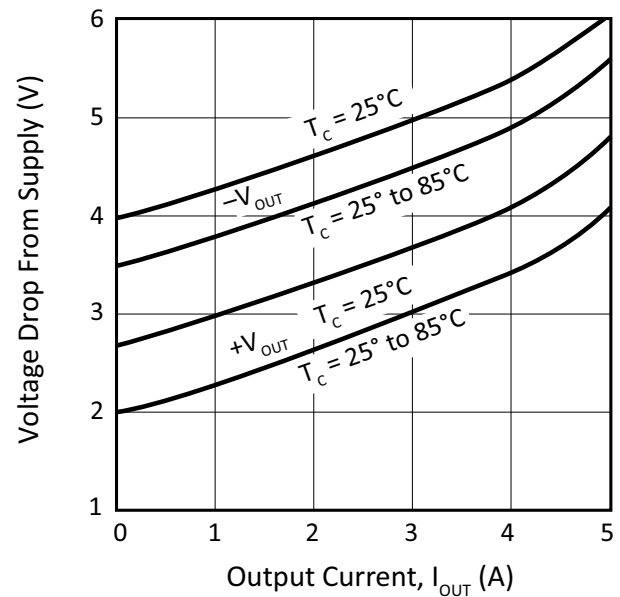


Figure 15: Output Voltage Swing



## SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.

The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads.

1. For DC outputs, especially those resulting from fault conditions, check worst case stress levels against the SOA graph.

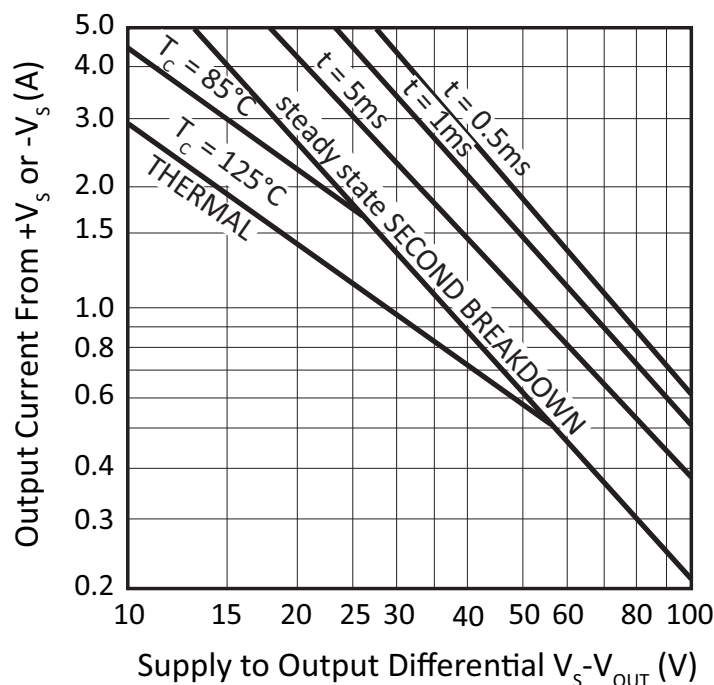
Make sure the load line does not cross the 0.5ms limit and that excursions beyond any other second breakdown line do not exceed the time label, and have a duty cycle of no more than 10%.

A Spice type analysis can be very useful in that a hardware setup often calls for instruments or amplifiers with wide common mode rejection ranges. Please refer to Application Notes, AN01 and AN22 for detailed information regarding SOA considerations.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at  $T_C = 85^\circ\text{C}$ :

$\pm V_S$	Short to $\pm V_S$ C, L, or EMF Load	Short to Common
50V	0.21A	0.61A
40V	0.3A	0.87A
35V	0.36A	1.0A
30V	0.46A	1.4A
25V	0.61A	1.7A
20V	0.87A	2.2A
15V	1.4A	2.9A

Figure 16: SOA



## GENERAL

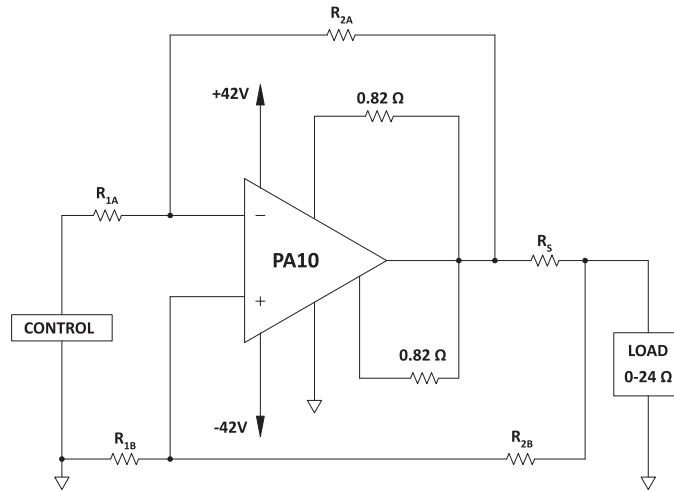
Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit [www.apexanalog.com](http://www.apexanalog.com) for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

## TYPICAL APPLICATION

DC and low distortion AC current waveforms are delivered to a grounded load by using matched resistors (A and B sections) and taking advantage of the high common mode rejection of the PA10.

Foldover current limit is used to modify current limits based on output voltage. When load resistance drops to 0, the current is limited based on output voltage. When load resistance drops to 0, the current limit is 0.79A resulting in an internal dissipation of 33.3W. When output voltage increases to 36V, the current limit is 1.69A. Refer to Application Note 9 on foldover limiting for details.

Figure 17: Typical Application (Voltage-to-Current Conversion)



## CURRENT LIMITING

Refer to Application Note 9, “Current Limiting”, for details of both fixed and foldover current limit operation. Beware that current limit should be thought of as a  $\pm 20\%$  function initially and varies about 2:1 over the range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

For fixed current limit, leave pin 7 open and use equations 1 and 2.

1.

$$R_{LIM}(\Omega) = \frac{0.65V}{I_{LIM}(A)}$$

2.

$$I_{LIM}(A) = \frac{0.65V}{R_{LIM}(\Omega)}$$

Where:

$I_{LIM}$  is the current limit in amperes.

$R_{LIM}$  is the current limit resistor in ohms.

For certain applications, foldover current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum foldover slope, ground pin 7 and use equations 3 and 4.

3.

$$I_{LIM}(A) = \frac{0.65V + (V_{OUT} \cdot 0.014)}{R_{LIM}(\Omega)}$$

4.

$$R_{LIM}(\Omega) = \frac{0.65V + (V_o \cdot 0.014)}{I_{LIM}(A)}$$

Where:

$V_{OUT}$  is the output voltage in volts.

Most designers start with either equation 1 to set  $R_{LIM}$  for the desired current at 0V out, or with equation 4 to set  $R_{LIM}$  at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor ( $R_{FO}$ ) between pin 7 and ground. Use equations 4 and 5 with this new resistor in the circuit.

5.

$$I_{LIM}(A) = \frac{0.65V + \frac{V_{OUT} \cdot 0.14}{10.14 + R_{FO}}}{R_{LIM}(\Omega)}$$

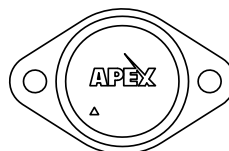
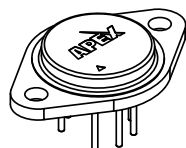
6.

$$R_{LIM}(\Omega) = \frac{0.65V + \frac{V_{OUT} \cdot 0.14}{10.14 + R_{FO}}}{I_{LIM}(A)}$$

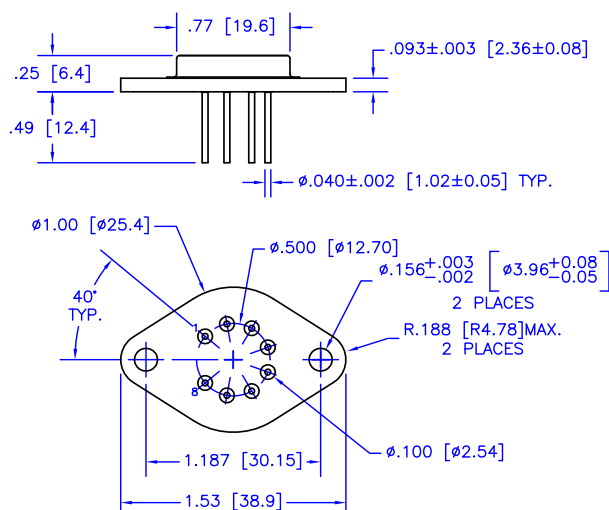
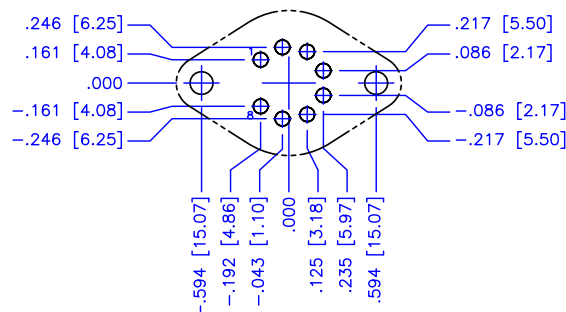
Where:

$R_{FO}$  is in K ohms.

## PACKAGE STYLE CE



### Ordinate dimensions for CAD layout



**NOTES:**

1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Header flatness within pin circle is .0005" TIR, max.
4. Header flatness between mounting holes is .0015" TIR, max.
5. Standard pin material: Solderable nickel-plated Alloy 52.
6. Header material: Nickel-plated cold-rolled steel.
7. Welded hermetic package seal
8. Isolation: 500 VDC any pin to case.
9. Package weight: .53 oz [15 g]

**NEED TECHNICAL HELP? CONTACT APEX SUPPORT!**

For all Apex Microtechnology product questions and inquiries, call toll free 800-546-2739 in North America. For inquiries via email, please contact [apex.support@apexanalog.com](mailto:apex.support@apexanalog.com). International customers can also request support by contacting their local Apex Microtechnology Sales Representative. To find the one nearest to you, go to [www.apexanalog.com](http://www.apexanalog.com)

## IMPORTANT NOTICE

Apex Microtechnology, Inc. has made every effort to insure the accuracy of the content contained in this document. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (expressed or implied). Apex Microtechnology reserves the right to make changes without further notice to any specifications or products mentioned herein to improve reliability. This document is the property of Apex Microtechnology and by furnishing this information, Apex Microtechnology grants no license, expressed or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Apex Microtechnology owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Apex Microtechnology integrated circuits or other products of Apex Microtechnology. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

APEX MICROTECHNOLOGY PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED TO BE SUITABLE FOR USE IN PRODUCTS USED FOR LIFE SUPPORT, AUTOMOTIVE SAFETY, SECURITY DEVICES, OR OTHER CRITICAL APPLICATIONS. PRODUCTS IN SUCH APPLICATIONS ARE UNDERSTOOD TO BE FULLY AT THE CUSTOMER OR THE CUSTOMER'S RISK.

Apex Microtechnology, Apex and Apex Precision Power are trademarks of Apex Microtechnology, Inc. All other corporate names noted herein may be trademarks of their respective holders.